Development and Realization of Camera Electronics for Space-based Ultra-High-Energy Cosmic Ray Detectors

Dissertation

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Zusammenfassung

Die Entdeckung der kosmischen Strahlung vor über 100 Jahren führte zu zahlreichen Errungenschaften in der Teilchenphysik, da hierdurch eine natürliche Teilchenquelle verfügbar war, mit Energien, welche mit Beschleunigern auf der Erde nicht erreichbar waren. Obwohl die höchsten je gemessenen Energien der kosmischen Strahlung noch immer nicht im Labor erzeugt werden können, sind es heutzutage eher die Fragen aus dem Bereich der Astronomie, welche hierbei von Interesse sind.

Dabei ist es gerade die kosmische Strahlung mit der höchsten Energie, welche dabei helfen soll, die sehr grundlegenden aber noch immer ungeklärten Fragen zu beantworten: Woher stammt sie? Wie werden die Teilchen zu solch hohen Energien beschleunigt? Wie ist ihre Zusammensetzung?

Aufgrund des äußerst geringen Flusses von ungefähr einem Teilchen pro km^2 und Jahrhundert bei Energien von $10^{20}\,\mathrm{eV}$ müssen die Experimente, welche der Erforschung von kosmischer Strahlung dienen, riesige Flächen überspannen, um in akzeptabler Zeit eine ausreichende Anzahl von Teilchen zu detektieren.

JEM-EUSO ist ein Missionskonzept, welches das Potential hat, die Detektorfläche der größten aktuell operierenden Experimente um eine Größenordnung zu erhöhen. Durch ein Teleskop im Weltraum, welches die Erdatmosphäre beobachtet, können die schwachen Lichtsignale der Teilchenschauer aufgezeichnet werden. Diese entstehen, wenn ein hoch-energetisches kosmisches Teilchen auf ein Molekül der Atmosphäre trifft und sich dadurch ein ausgedehnter Luftschauer ausbildet.

Im Rahmen dieser Arbeit habe ich experimentelle Studien durchgeführt, welche für solch ein Weltraumteleskop essentiell sind. Im Speziellen habe ich zwei zentrale Komponenten der digitalen Kameraelektronik entwickelt, deren Hauptaufgaben darin bestehen, die anfallende Datenrate um insgesamt neun Größenordnungen zu reduzieren: das ‘Cluster Control Board (CCB)’ und das ‘Photo-Detector Module (PDM) Control Board’. Dabei verwaltet und kombiniert das CCB die Daten von einer Gruppe von PDMs – welches die grundlegende Einheit des Detektors darstellt –, evaluiert einen Trigger-Algorithmus und sendet die Daten zum zentralen Missionscomputer. Die Hauptaufgabe des ‘PDM Control Board’ besteht darin, die analoge Elektronik der Kamera auszulesen und einen weiteren Trigger-Algorithmus auszuführen.

Die Arbeit beinhaltete die gesamte Entwicklung der Elektronik. Angefangen mit der Definition der Anforderungen, bis hin zur Entwicklung und dem Testen von Prototypen. Das Hauptziel war dabei stets die Demonstration der Funktionalität und der technischen Einsatzbereitschaft. Dieses Ziel konnte erreicht werden, indem die entwickelten Komponenten in verschiedenen, wegweisenden Projekten integriert wurden: EUSO-TA, ein bodengestütztes Teleskop, welches in der Wüste von Utah betrieben wurde; EUSO-Balloon, welches mit Hilfe eines Stratosphären-Ballons an den Rand des Weltraums gebracht wurde und erfolgreich das Beobachtungsprinzip demonstrierte; und EUSO-SPB, welches das automatische Aufzeichnen von Ereignissen demonstrierte, während es 12 Tage lang an einem Überdruck-Ballon am Rand zum Weltraum betrieben wurde.

Die erfolgreiche Entwicklung der Komponenten und die Implementierung der Trigger-Algorithmen stellt Technologie zur Verfügung, welche von jedem zukünftigen Projekt genutzt werden kann, um die hoch-energetische kosmische Strahlung vom Weltall aus zu erforschen. Solch ein weltraumgestütztes Teleskop wird ein neues Fenster in der Wissenschaft öffnen: Astronomie mit Hilfe von Teilchen.

Abstract

The discovery of cosmic rays more than 100 years ago led to several achievements in particle physics, as they provided a natural particle source at energies not accessible by accelerators in the laboratory. While this is still valid for the highest energies measured, the topics of interest are nowadays related to astronomy.

It is especially the Ultra-High-Energy Cosmic Rays (UHECRs) which will help to solve their most basic, yet unsolved, questions: Where are they from? How are they accelerated? What is their composition? Due to the extremely low flux of around 1 particle per km^2 and century at energies around 10^{20} eV, experiments have to be of large extend in order to gather enough statistics within an acceptable time frame.

JEM-EUSO is a mission concept which has the capability to increase the exposure of the largest currently operating projects by one order of magnitude. Placing a large field of view telescope into space and monitoring the Earth's atmosphere allows to observe the faint light signatures, which are generated when an UHECR interacts with a molecule of the atmosphere and an Extensive Air Shower is being formed.

In the context of this thesis, I have conducted experimental studies essential for such a space-based telescope. Specifically, I have developed two key components of the digital camera electronics, whose main tasks are the reduction of the data rate by nine orders of magnitude in total: the Cluster Control Board (CCB) and the Photo-Detector Module (PDM) control board. The CCB manages and combines the data from a cluster of PDMs, the basic detector unit, performs the second level trigger and transfers the data to the main mission computer. The PDM control board mainly interfaces the analog read-out electronics and performs the first level trigger.

The work covered the full development of the electronics. From the definition of the requirements to the development and testing of prototypes, with the aim of demonstrating the functional and technological readiness. This final goal was achieved by integrating the developed components into several pathfinder projects: EUSO-TA, which is a ground based instrument operated in the desert of Utah; EUSO-Balloon, which was brought to near space on board of a stratospheric balloon and demonstrated the observation principle; and EUSO-SPB, which demonstrated the self triggering capabilities during 12 days of operation on board a super-pressure balloon.

The successful development of the hardware and the implementation of the trigger algorithms provide technology suitable for any future mission devoted to the detection and observation of UHECRs from space. Such a space-based mission will open a new scientific window: astronomy through the particle channel.

Contents

1 Introduction to Cosmic Rays

The discovery and consequently the scientific investigation of Cosmic Rays (CRs) started in the early 20th century, triggered by the discovery of radioactivity. CRs were originally detected via the discharge of electroscopes – an observation which was wrongly interpreted to originate entirely from the ionizing radiation produced by radioactive materials in the Earth's crust. After several balloon flights in 1912, Victor Hess concluded that this ionizing radiation could not originate from the Earth, but penetrated the atmosphere from above, since its intensity did not decrease with increasing altitude, as expected of a radiation of terrestrial origin, but rather on the contrary increased with altitude.

In these experiments, Hess could also exclude the Sun as a source for the 'hypothetical radiation', as it was called in those days, since no reduction during night nor during a solar eclipse could be detected (Hess, 1912). The term 'radiation' is still used today, although CRs are now known to consist of particles and not of electromagnetic radiation like γ-rays or X-rays.

Further progress in the investigation of CRs was obtained with the invention of new detector types, the Geiger-Müller detectors, while the introduction of the concept of detectors in 'coincidence' (Rossi, 1930) allowed the study of single events.

By using cloud chambers, it became obvious that CRs consist of charged particles, which was first recognized by Skobelzyn, 1929 and investigated in more detail by Blackett et al., 1933 and Rieder et al., 1934. Soon after, it was found that rather distant Geiger-Müller counters are still triggering in coincidence (Kolhörster et al., 1938; Schmeiser et al., 1938), which eventually led to the concept of Extensive Air Showers (EASs): the primary CR impinges the Earth's atmosphere and creates a CR-induced particle shower. After this discovery, scientists started to focus also on the detection and investigation of EASs.

Since it was found that EASs could extend up to 300 m (Auger et al., 1939) when they reach the ground, it was deduced that the primary particle energies should be of the order of 10^{15} eV, and the flux was estimated to be 10^{-9} particles/min/cm^2 above 10^{15} eV.

The existence of these extraterrestrial high-energetic particles can be considered as the direct proof that astronomical sources are able to accelerate charged particles to extremely high energies. However, the discovery of CRs as a natural source of extremely high-energetic particles opened a wide field of new research, and allowed a series of breakthroughs in particle physics, until the accelerator technology for this energy range became available decades later, in 1953. This entirely new area of investigation led to several milestones in particle physics, like the discovery of the positron (Anderson, 1932, 1933), the muon (Anderson et al., 1936) and, years later, the charged and neutral kaons (Rochester et al., 1947), and the pion (Lattes et al., 1947a,b). Thus, Victor Hess' first detection of CRs was not only a significant discovery for astrophysics, but also led to new achievements in other scientific areas of research.

In this chapter, the detected spectrum of the CRs is introduced, and different spectral features are discussed. Special emphasis is given to Ultra-High-Energy Cosmic Rays (UHECRs), the topic of this thesis, and the research status of their properties like composition, production, and origin is described. In the last part of the chapter, the detection method for UHECRs, based on EASs, is explained.

1.1 The Cosmic Ray Spectrum

To understand the spectrum, origin and composition of CRs, the EASs (see also Section 1.3) were investigated by installing large detector arrays (like the air shower array 'Volcano Ranch'-experiment[1]), and the first CR with an energy of 10^{20} eV was recorded in 1962 by John Linsley and Livio Scarsi (Linsley, 1963). The CR spectrum (see Fig. 1.1) as measured by many different experiments can be described as a broken power law in the form of

$$\Phi_{CR}(E) \propto E^{-\alpha}, \tag{1.1}$$

with the flux Φ_{CR} as a function of the energy E and the power-law index α. The spectrum spans over a wide energy range and contains several features at which the power-law index α changes, indicating different types of sources of CRs, at different energies:

- Below $E \leq 10^9$ eV, the measured spectrum is dominated by the solar wind component and thus follows the solar variation.
- In the energy range from 10^9 eV to 10^{15} eV, a power-law index of $\alpha = 2.7$ can be found (Blümer et al., 2009), and the flux decreases from ~ 1000 particles/m^2/s to ~ 1 particle/m^2/year.
- The 'Knee' of the spectrum – its most prominent feature – can be found around $\sim 10^{15}$ eV.

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[1] The MIT Volcano Ranch Air Shower array was composed of 19 scintillation detectors arranged on a surface of 2 km^2 to detect the secondary particles coming from the EAS (Linsley et al., 1961).

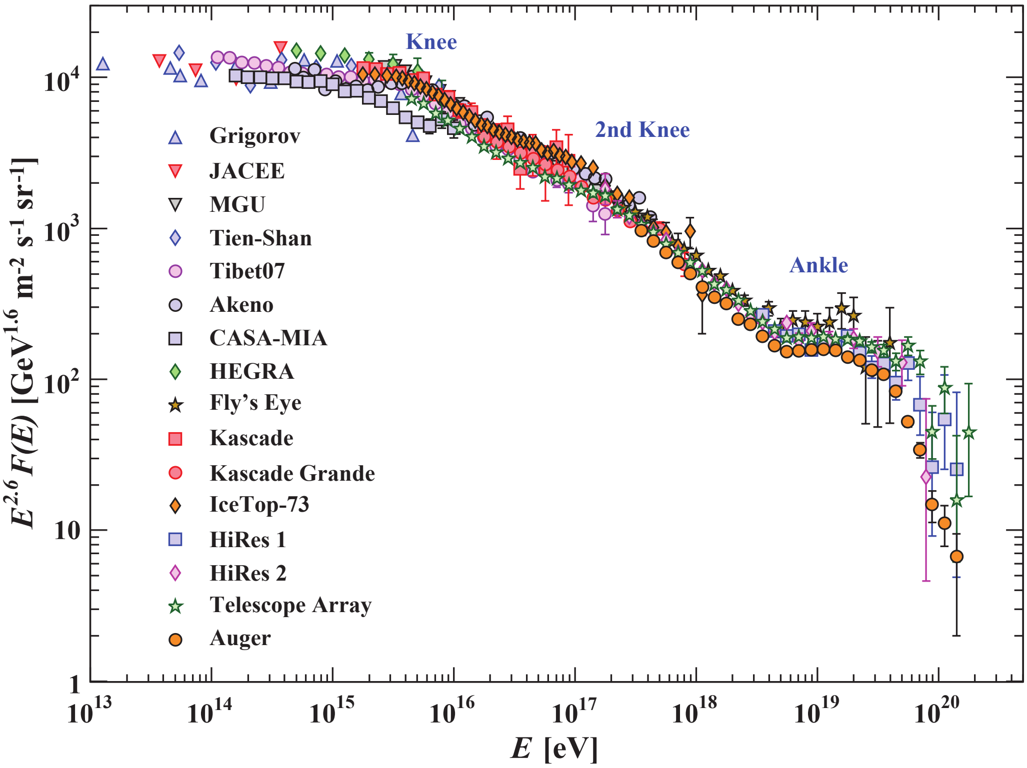

Figure 1.1: The all-particle CR spectra recorded with the main experiments is showing the two most prominent features ('Knee' and 'Ankle'), where the slope of the spectra changes. By scaling the measured flux with the energy (multiplied here by $E^{2.6}$), the more subtle features like the '2nd Knee' become apparent. The statistics of the high-energy part of the spectra are still very low. (Figure: Tanabashi et al., 2018)

- After this 'Knee', the spectrum becomes steeper, with α changing to $\alpha = 3.1$ (Blümer et al., 2009).
- The installation of even larger particle detector arrays and the first fluorescence light telescope – called the 'Fly's Eye'[2] – gave further access to the higher energy end of the spectrum and another feature was established in the early 1990s:
  At an energy around $10^{18.6}$ eV, the spectrum hardens again and goes back to an index of $\alpha = 2.7$ – this feature is commonly referred to as the 'Ankle'.

CRs with energies beyond the 'Ankle' are referred to as UHECRs. Their flux drops to around 1 particle per km^2 and year, and at the highest energies around 10^{20} eV,

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[2] Fly's Eye is an experiment composed of 67 fluorescence telescopes which are pointing at different locations in the sky to provide a full sky coverage.

only around 1 particle per km^2 and century is detected.

The described spectral features reflect various aspects of the CR production as well as their distribution and propagation to Earth. After re-scaling the flux with a power of the energy, these features in the spectrum are getting pronounced, and even more subtle features become visible like the '2nd Knee'. While there are several theories on the origin of the various spectral features – which are still under discussion – the most accepted explanations shall be discussed in the following.

1.1.1 The 'Knee'

According to the most popular theory, the existence and position of the 'Knee' in the measured CR spectrum is associated with the maximum energy E_{max} of charged particles which are accelerated in the shock fronts of Galactic supernovae (see Section 1.2.2), which leads to a decrease in the flux, when this component dies out.

The second most prominent explanation for the 'Knee' is the 'leakage' model whose explanation is based on the fact that the higher energy CRs are not confined in the Galactic magnetic field anymore. Thus, they escape the Milky Way, which explains the decrease of detected particles at this energy (see Section 1.2.3, Giacinti et al., 2015). On the other hand, this also implies that CRs with energies up to the 'Knee' are supposed to be of Galactic origin due to their confinement in the Galactic magnetic field.

Both explanations additionally imply that the 'Knee' originates from the cut-off connected to protons with $E^p_{max} = 4.5 \times 10^{15}\,\mathrm{eV} = 10^{15.6}\,\mathrm{eV}$, while the steepening of the spectrum after the 'Knee' is a result of the subsequent cut-offs associated with the E_{max} for heavier elements.[3] This idea was strengthened, when the detection of an 'Iron Knee' was reported at an energy of $10^{16.9}\,\mathrm{eV}$ (Apel et al., 2011) which fits quite well to the energy limit expected for iron: $E^{Fe}_{max} = 26 \cdot E^p_{max} = 10^{17.1}\,\mathrm{eV}$. In this picture, the '2nd Knee' at $10^{17.6}\,\mathrm{eV}$ could then fit to the last cut-off from the heaviest (stable) particles, which is at $92 \cdot E^p_{max} = 10^{17.6}\,\mathrm{eV}$ (Hörandel, 2003). On the other hand, the transition from Galactic to extragalactic CRs is assumed to happen between $10^{17}\,\mathrm{eV}$ and $10^{18}\,\mathrm{eV}$, while the exact energy is not known yet.

1.1.2 The 'Ankle'

The 'Ankle' feature of the spectrum might be explained by the appearance of an extragalactic component with a harder spectrum (Tanabashi et al., 2018). While

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[3] Elements with a larger atomic number Z and their larger electrical charge are stronger confined by a magnetic field than protons, i.e., particles with higher Z possess a smaller Larmor radius r_{Larmor} than protons. Thus, they need a higher energy to escape the Galactic magnetic field, but also the maximum energy E_{max} to which they can be accelerated is higher than E^p_{max}.

the most popular explanations for the ‘Knee’ favor particles of Galactic origin, this feature of the spectrum might account for the extragalactic particles of the CRs, since no Galactic sources are known up to date which might provide charged particles with an energy higher than that of the ‘Knee’.

1.1.3 High-energy cut-off

Finally, the spectrum cuts off at around $10^{19.7}$ eV, which is explained by the interaction of the UHECR protons with photons of the Cosmic Microwave Background Radiation (CMBR). An upper energy limit is produced in the spectrum by considering the excitation of a Δ^+ resonance in proton photon interactions. The proton will quickly lose energy, producing the spectral feature called the Greisen-Zatsepin-Kuzmin (GZK) cut-off, that will be discussed in more detail in Section 1.2.3.

1.2 Ultra-High-Energy Cosmic Rays

As the topic of this thesis is the detection and investigation of the highest energetic CRs, this section discusses these UHECRs in more detail.

1.2.1 Composition

The composition of UHECRs is still unknown and a key topic of current research. While a direct measurement of the particles above the atmosphere is feasible at low energy[4] – currently up to energies around 10^{14} eV – UHECRs can only be detected indirectly, as their very low flux of less than 1 particle/km^2/year at the ‘Ankle’ leaves their direct detection unfeasible. Thus, detailed studies on the CR composition are only available for the low-energy part of the spectrum[5], while not much is known about the composition of UHECRs. In addition to the low flux, the indirect measurement imposes difficulties on the interpretation of the data, as it strongly depends on

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[4] Two balloon based experiments from the 1990s delivered the highest-energy data on directly measured CRs up to now. The Japanese-American Cooperative Emulsion Experiment (JACEE) was a series of balloon flights between 1979 and 1995 and measured the CR spectra up to 8×10^{14} eV (Asakimori et al., 1998). The RUssia Nippon JOint Balloon (RUNJOB) had 10 successful flights between 1995 and 1999 with a similar energy range and measured one proton with an energy of 10^{15} eV which is the highest energy of a proton measured directly (Hareyamaa et al., 2006).

[5] The abundances of low-energy CRs around 10^9 eV follows basically the abundances of the solar system. Nevertheless, a few elements are more abundant in CRs which are assumed to be the result of spallation processes from C, N, O, Fe, and Pb during their propagation to Earth (see Blümer et al., 2009).

the particular model used to calculate the interactions within the atmosphere (see also Section 1.3). This leads to large uncertainties, and it is already challenging to separate the composition into low- and high-mass CRs. While for energies around 10^{17} eV, an iron dominated composition has been found (see also the 'Iron Knee' in Section 1.1.1), which changes to a light composition (proton dominated) between 10^{18} eV to 10^{19} eV, there is still a large uncertainty in the composition at energies above 10^{19} eV (see Hanlon, 2018).

1.2.2 Production

As UHECRs require a powerful source in order to obtain their enormous energies, supernova explosions were soon discussed as their possible sources. The energy density of the CRs can be estimated to be around $\rho_{CR} \approx 1\,\mathrm{eV\,cm^{-3}}$ – an energy density for which only 10 % to 20 % of the energy released in a supernova is required (Lipari, 2008), considering a typical rate of about three supernovae per century in a typical galaxy. Furthermore, the power-law components of the CR spectrum indicate a non-thermal acceleration process. The most-accepted explanation on the acceleration of CRs is based on the original idea from Fermi in 1949, and has been suggested in the late 1970s by 1977, Krymskii, 1977, Bell, 1978a,b and Blandford et al., 1978.

A new version of the process has been further developed and refined over the years, and is nowadays known as the first-order Fermi mechanism or diffusive shock acceleration. In this process, the increase in energy of the accelerated particles is proportional to the ratio between the shock velocity and the speed of light: $\Delta E \propto \beta_s = \frac{v_s}{c}$.[6] The first-order Fermi mechanism is a statistical process that applies to strong, collision-less[7] shock fronts with an inhomogeneous magnetic field, as found in supernova remnants. By diffusive scattering in the inhomogeneous magnetic fields present upstream of the shock, i.e., in the un-shocked medium, and downstream of the shock, i.e., in the shocked medium, a high-energetic charged particle can gain energy each time it crosses the shock front. The energy gain of a particle per round trip – i.e., crossing the shock front twice – is proportional to its energy: $\Delta E \propto E$. Therefore, the final energy of the particle depends on how often it crosses the shock front, which depends on the time it is confined in the region, i.e., on the probability

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[6] The original process is nowadays referenced to as the second-order Fermi mechanism since the increase in energy is $\Delta E \propto \beta_s^2$ and therefore less efficient.

[7] A collision-less shock front is defined as a shock front which propagates into a medium for which the mean free path of the particles is much larger than the width of the shock. Thus, the particles are not thermalized during the shock, so that some particles will keep their very high energies which they obtained during the shock, due to the low number of Coulomb collisions. Instead the magnetic field dominates the interaction of the particles.

that the particle can escape.

The maximum energy the particle can reach via the Fermi mechanism can be estimated by

$$E_{max} \propto Ze \cdot \beta_s \cdot B \cdot R_s \,, \tag{1.2}$$

with Ze representing the charge of the particle, B the magnetic field of the region, β_s the velocity of the shock in terms of the speed of light ($\beta_s = \frac{v_s}{c}$), and $R_s = t \cdot v_s$ the size of the shock region with t being the lifetime of the shock.

Using this estimate, the typical maximum energy of particles accelerated by a certain astronomical source can be calculated. The 'Hillas' plot (see Figure 1.2) shows different types of astronomical objects plotted with respect to their magnetic field strength and typical size. Using Equation 1.2, the maximum energy to which a charged particle can be accelerated can then be added to the plot and possible sources can be identified. In this diagram, E_{max} is basically a diagonal line and its position depends on the particle (i.e., on its charge) and the velocity of the shock region β_s which also can be regarded as a factor for the effectiveness of the acceleration. The solid line given in Figure 1.2 shows what size and magnetic field strength are needed to accelerate a proton to 10^{20} eV, while the dashed line accounts for more realistic shock velocities – this means all sources to the right of the corresponding lines are able to accelerate a proton to $E^p_{max} = 10^{20}\,\mathrm{eV}$. The dotted line shows the same for the energy $E^p_{max} = 10^{14}\,\mathrm{eV}$. As it can be seen from the dotted line, supernova remnants are a promising galactic source for CRs up to the 'Knee' of the CRs spectrum. In this simple picture, typical values for supernovae (Lipari, 2008) result in

$$E_{max} \propto Ze \cdot \beta_s \cdot B \cdot R_s \approx Z \cdot 0.4 \times 10^{14}\,\mathrm{eV} \cdot \left(\frac{\beta_s}{0.03}\right) \cdot \left(\frac{B}{3\,\mu\mathrm{G}}\right) \cdot \left(\frac{R_s}{5\,\mathrm{pc}}\right) \tag{1.3}$$

Further developments of the original Fermi mechanism suggest that the accelerated charged particle itself – which is also inducing a magnetic field – could interact and amplify the ambient magnetic field and therefore lead to even higher energies. Calculations show that the magnetic field can be a factor of 1000 higher – which leads to maximum energies of up to $E_{max} \approx Z \cdot 10^{17}\,\mathrm{eV}$ (Lucek et al., 2000).

1.2.3 Origin and Propagation

In order to obtain more insight into the origin of the particles and their impact on the features of the spectrum, two considerations for Galactic and extragalactic particles shall be discussed in this section.

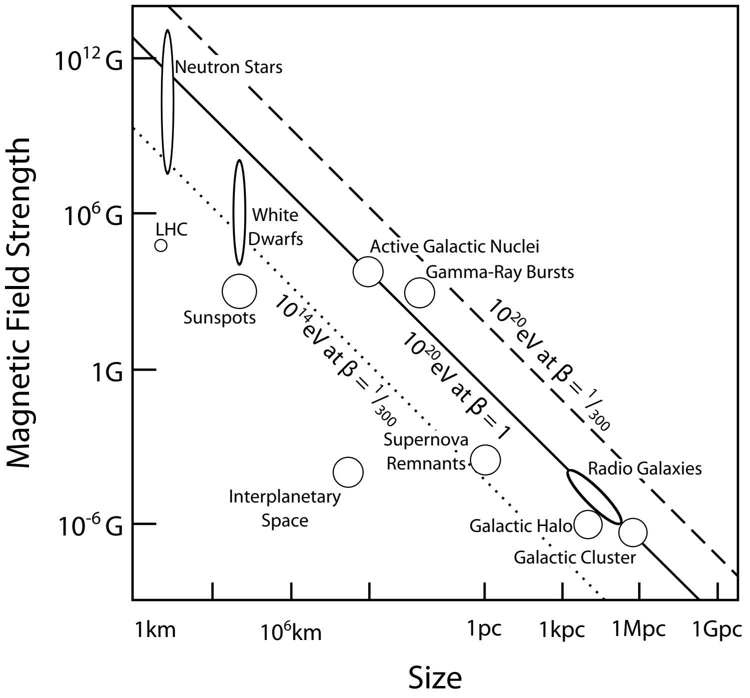

Figure 1.2: In the Hillas plot, different astronomical sources are plotted with respect to their size and magnetic field strength. The diagonal lines mark the limit at which a source is capable to accelerate particles to an energy of 10^{14} eV (dotted line) and 10^{20} eV (solid line and dashed line): only sources which lie to the right of the respective line can create such high-energetic particles. The lines are plotted for different values of β, which represents the effectiveness of the acceleration mechanism. (Image based on: Hillas, 1984 and JEM-EUSO Collaboration, 2010)

1.2.3.1 Galactic Cosmic Rays

For the origin of CRs, we need to consider that up to a certain energy limit, charged particles are confined within the Galaxy, due to the Galactic magnetic field. With a simple calculation of the Larmor radius for a charged particle in a (uniform) magnetic field

$$r_{\text{Larmor}} = \frac{E}{ZeB} \approx \frac{1}{Z} \cdot \left(\frac{E}{10^{18}\,\text{eV}}\right) \cdot \left(\frac{\mu\text{G}}{B}\right) \text{kpc}\,, \tag{1.4}$$

it can be calculated that the Larmor radius for a proton at an energy of 10^{18} eV is of the order of 1 kpc and therefore, comparable to the thickness of the Milky Way. Thus, CRs have an increasing probability to escape the magnetic field of the Milky Way with increasing energy. In addition, it is expected that at a certain energy, an extragalactic CR component appears. Both effects could lead to a change in the slope of the spectrum, but it is still under discussion which feature corresponds to which effect. Nevertheless, it is commonly accepted that UHECRs are extragalactic simply due to their large Larmor radii.

1.2.3.2 Extragalactic Cosmic Rays

In 1966, Kenneth Greisen (Greisen, 1966), Vadim Kuz'min and Georgiy Zatsepin (Zatsepin et al., 1966) independently calculated an energy limit for high-energy protons from distant sources based on the interaction with the CMBR, also known as the 'GZK cut-off'.

Through this interaction, the particle permanently loses energy, until its remaining energy is too low to trigger further interactions. Thus, ultra-high-energy protons could reach us from a maximal horizon, and this provides additional information about the origin of the particle.

In the following, the two processes which can be triggered through the interaction of the CRs with the CMBR are discussed: the excitement of a Δ^+ resonance and electron-positron pair-production.

Δ^+ resonance excitation: A high-energy proton can be excited to its first state by a photon from the CMBR to form a Δ^+ resonance. This resonance will then decay, through which the proton loses around 20 % (Zatsepin et al., 1966) of its initial energy:

$$\begin{aligned} p + \gamma_{2.7\,\mathrm{K}} \rightarrow \Delta^+ &\rightarrow p + \pi^0 \\ &\rightarrow n + \pi^+ . \end{aligned}$$

If, after this process, the energy of the proton is still above the threshold energy to form a Δ^+ resonance, which is

$$E_{\mathrm{th}}^{\pi} \approx 5 \times 10^{19}\,\mathrm{eV}\,,$$

it can undergo successive interactions and gradually lose energy until its energy is below E_{th}^{π}.

This energy loss is directly connected to a maximum propagation distance for the highest-energy protons. With the density of the CMBR photons[8] and their cross section[9] for this interaction, it can be calculated that the proton energy will fall below E_{th}^{π} within 100 Mpc, which basically does not depend on the initial energy of the proton (see Figure 1.3, left).

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[8] $\rho_{\gamma_{2.7\,\mathrm{K}}} \approx 410\,\mathrm{cm}^{-3}$ (Bennett et al., 2003)

[9] The mean cross section is about 200 µb (Greisen, 1966).

e^+e^- pair-production: A second mechanism through which the proton will lose energy is pair production. In this process, an electron-positron pair is created after the photon of the CMBR interacts with the proton:

$$p + \gamma_{2.7\,\mathrm{K}} \rightarrow p + e^+e^- \,.$$

Energy- and momentum-conservation can only be satisfied if the proton receives some recoil, thus losing energy. Due to the high mass difference between proton and electron, this energy loss is very small and needs long propagation distances to be effective. The energy threshold for this process lies at

$$E_{th}^{e^+e^-} \approx 7 \times 10^{17}\,\mathrm{eV}\,.$$

In conclusion, two features in the extragalactic proton spectra are expected due to these mechanisms (see Figure 1.3, right):

- a weak suppression of the flux at energies around 7×10^{17} eV based on the less effective pair production,
- and a strong steepening around 5×10^{19} eV, based on the excitation of the Δ^+ resonance – the 'GZK-cutoff'.

This implies that the sources for CRs with energies above 5×10^{19} eV should be located within a ~ 100 Mpc sphere: the 'GZK-sphere'. It is expected that the sources which can accelerate CRs to these energies follow the anisotropic (baryonic) matter distribution, and therefore, it is assumed that the arrival directions of the UHECRs are anisotropic, too.

1.2.4 Anisotropy

As already discussed in Section 1.2.3, the Larmor radius of low-energy CRs is small compared to the size of the Galaxy and thus they are confined inside the Galactic magnetic field. This also implies that the information of their origin is lost (or impossible to reconstruct) and the arrival direction is basically isotropized. Nevertheless, large scale anisotropies at lower energies could be used to improve the knowledge on the Galactic magnetic field.

On the contrary, the UHECRs are deflected only slightly and could be used to identify their sources by searching for anisotropies in the flux of the highest energies. In addition, the GZK-effect imposes an additional constraint on possible sources. While events from sources at large distances would overlap, this will be unlikely for sources within the GZK-sphere (see Section 1.2.3).

Recently, the two largest experiments currently operating have reported a 'hot-spot' in the northern sky (Abbasi et al., 2014) and a 'warm-spot' in the southern sky (Aab

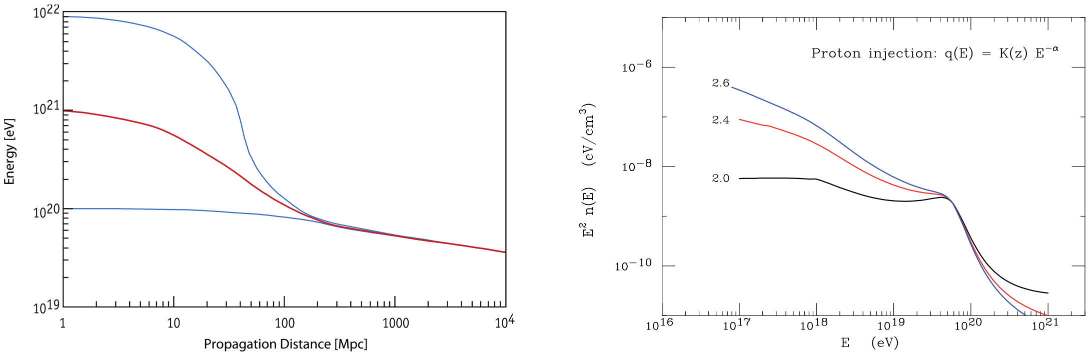

Figure 1.3: A high-energy proton can interact with the CMBR and form a Δ^+ resonance. The subsequent decay leads to an energy loss of the proton, whose energy drops to around 10^{20} eV within 100 Mpc. This propagation distance is nearly independent of the initial energy (left image based on: Aharonian et al., 1994). The resulting effect, is a steepening in the observable spectra at an energy of 5×10^{19} eV – also called GZK-cutoff. This can be seen in the calculated spectra on the right (shown for three different injection power-law indices). Another steepening can be found at an energy of 7×10^{17} eV which is caused by pair-production (right image based on: Lipari, 2008).

et al., 2015). Both searches were done with UHECRs of energies above 57×10^{18} eV and 58×10^{18} eV respectively. While the 'warm-spot' matches with Centaurus-A – the nearest radiogalaxy at a distance of 3.8 Mpc – this correlation is statistically not significant[10]. The 'hot-spot' on the other hand is statistically significant and coincidences with M82 – a spiral galaxy at a distance of 3.5 Mpc[11].

1.3 Detection of Cosmic Rays using Extensive Air Showers

The steep decrease in the CR flux for higher energies (see Figure 1.1) makes the experimental setups for the detection of CRs more and more challenging with increasing particle energy. Due to the low flux of only 1 particle/km^2/century at 10^{20} eV, wide collecting area experiments are required to access the high-energy part of the spectrum. While in order to measure the low-energy part of the spectrum it is still possible to deploy particle detectors in space or on balloons, and directly measure the primary CRs, this is not feasible for the UHECRs, due to the extremely low flux of the primary particles. Only indirect measurements with large detector arrays can lead

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[10] This 'warm-spot' has a 1.4 % probability to arise by chance from an isotropic distribution (Aab et al., 2015).

[11] This 'hot-spot' has a probability of 3.7×10^{-4} % to appear by chance in an isotropic distribution (Aab et al., 2015).

to relevant statistics of events. In these indirect measurements, secondary particles as well as their fluorescence light and possibly the Cherenkov light are detected and used to model the Extensive Air Showers (EASs), generated by the primary particles. The different physical processes which allow this indirect measurement are discussed in this section.

1.3.1 Creation of Extensive Air Showers

An UHECR which impinges the Earth's atmosphere eventually interacts with a nucleus after traveling a certain distance through the atmosphere. The average distance (or mean free path) is given by the cross section of the particle and depends strongly on the type of particle: a heavy nucleus will penetrate the atmosphere much less compared to a proton, and its first interaction will occur much higher in the atmosphere. This primary interaction produces additional particles, which is referred to as particle multiplication. This leads to a cascade of further interactions producing a shower of particles, fluorescence light, and – due to the high energy of the primary particle – also Cherenkov light[12], both in the UltraViolet (UV) energy range. This complex phenomenon is indeed what we call Extensive Air Shower.

1.3.2 Composition of Extensive Air Showers

EASs consist of a very large number of particles spread over a large area: e.g., a proton with an energy of 10^{19} eV which vertically enters the Earth's atmosphere produces around 3×10^{10} particles[13] at sea level from which 99 % are photons as well as electrons and positrons, with a ratio of 6:1 (carrying 85 % of the total energy). The remaining 1 % of the produced particles are muons (carrying around 10 % of the total energy) and pions (carrying around 4 % of the total energy), and finally, a few neutrinos and baryons. The footprint of the shower at sea level extends over a few km^2 (Letessier-Selvon et al., 2011).

In a simple picture, the first hadronic interaction mainly produces pions, and the development of the shower can be separated into three components (see Figure 1.4):

(i) the nucleon cascade formed by nuclear fragments, whereas subsequent interactions with air molecules are similar to the primary collision,

(ii) the pion cascade emerging the from charged pions $\pi^{\pm}$, reaching the ground as muons, and finally,

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[12] Since the shower develops faster than the speed of light in the atmosphere, Cherenkov light is produced.

[13] This includes only particles with an energy of more than 200 keV.

(iii) the electromagnetic cascade originating from the decaying neutral pions π^0, reaching the ground as photons, electrons, and positrons.

While the nucleon cascade (i) and the pion cascade (ii) are usually considered together as the *hadronic cascade*, (iii) represents the *electromagnetic component* of the shower. These cascades are discussed in the following sections.

Electromagnetic cascade The electromagnetic cascade is initialized by the decay of the neutral pions into two photons:

$$\pi^0 \rightarrow 2\gamma \, .$$

This main decay channel of the neutral pions has a probability of nearly 99 %, and a very short mean lifetime of the π^0 of 8.5×10^{-17} s. As long as their energy is high enough, the produced photons will mainly undergo pair production:

$$\gamma \rightarrow e^- + e^+ \, ,$$

and finally, the electron/positron will produce further photons via Bremsstrahlung and the process of pair production can start over forming the electromagnetic cascade. This process repeats as long as the individual energy of the electron/positron is above a critical energy at which the energy loss due to Bremsstrahlung is equal to the energy loss by ionization (which is around $E_c^\gamma = 80\,\mathrm{MeV}$ in air), i.e., absorption processes are dominating.

Hadronic cascade Some very basic properties of the hadron induced EAS can be deduced by extending a simple model developed by Heitler, 1954 for pure electromagnetic cascades (initiated by a high-energy CR photon). For this simple model, it is assumed that each hadronic interaction produces two charged and one neutral pion and that the energy is equally split. Thus, every pion carries $\frac{1}{3}$ of the initial energy. This means that with each interaction, $\frac{1}{3}$ of the energy goes directly into the electromagnetic cascade via the π^0, while $\frac{2}{3}$ are still available for further hadronic interactions. This process repeats until the pion energy is below a critical energy at which the decay into a muon and a neutrino

$$\pi^+ \rightarrow \mu^+ + \nu_\mu \text{ and}$$
$$\pi^- \rightarrow \mu^- + \bar{\nu}_\mu$$

is more likely than other competing interactions. This happens around $E_c^\pi = 20\,\mathrm{GeV}$ in air. At this point, the muons basically decouple from the shower and propagate to the ground with only a small energy loss, and are therefore sensitive to the characteristics of the hadronic interactions.

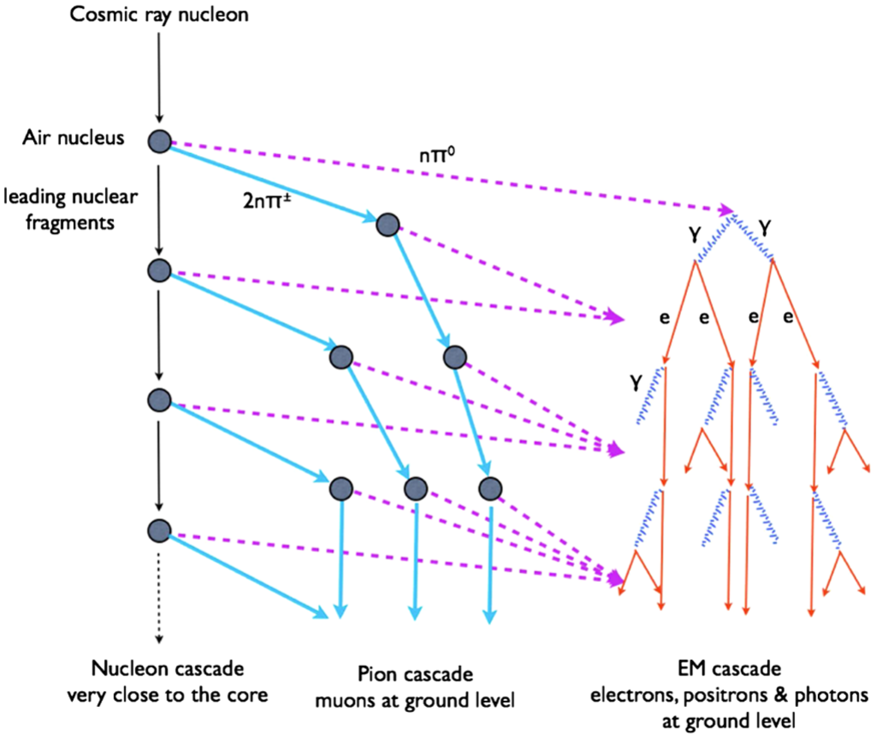

Figure 1.4: Basic scheme of the evolution of an EAS. In this simple picture, the EAS can be divided into three components: the nucleon cascade formed by nuclear fragments, the pion cascade arising from the charged pions, and the electromagnetic cascade arising from the neutral pions. The electromagnetic component carries the biggest part of the total energy, which is around 85 %. (Image: Letessier-Selvon et al., 2011)

Based on the repetition of this process, energy is transferred from the hadronic cascade into the electromagnetic component and after n interactions, the energy transfer can be described as

$$E_{had} = \left(\frac{2}{3}\right)^n \cdot E_0 \qquad \text{and} \qquad E_{em} = E_0 - E_{had}\,,$$

with E_{had} being the energy of the hadronic cascade, E_{em} the energy of the electromagnetic cascade, and E_0 the initial energy of the primary CR particle. The number of cycles n of pion generations can be determined by simulations and is most likely around 5 to 6 and increases slightly with energy (Blümer et al., 2009; Meurer et al., 2006). Therefore, around 85 % to 95 % of the energy of the initial particle is transported in the electromagnetic component at the highest energies. So the higher the energy of the primary particle, the more charged particles are available when the shower reaches its maximum and therefore, the more energy is lost due to ionization.

1.3.3 Detection of Extensive Air Showers

The – just described – energy loss due to ionization can be used to detect EASs: Mainly nitrogen molecules become ionized, as the major part of the air consists of nitrogen. When the ionized molecules relax again, fluorescence light is emitted in the UV range between 300 nm to 400 nm. It is this fluorescence light which is used to identify and detect EAS and thus UHECRs. In addition to the fluorescence light, also other secondary particles of the shower can be detected with on-ground detectors.

The key-parameters of an EAS which can be measured are

- the number of particles reaching the ground,
- the amount of fluorescence light, and
- the temporal and spatial evolution of the fluorescence light.

These parameters allow the reconstruction of the properties of the primary particle like its energy, type, and arrival direction, after fitting detailed empirical models and Monte-Carlo simulations of the shower development to the data. Through this, important information about the composition and the origin of UHECRs can be obtained, and candidates for their sources may be identified.

2 The JEM-EUSO Mission

The *Extreme Universe Space Observatory on board the Japanese Experiment Module* (JEM-EUSO) is the first space mission concept devoted to fundamental questions on UHECR physics:

- Where do they come from?
- How are they accelerated?
- What is their composition?

By looking down at the Earth's atmosphere, JEM-EUSO will record the fluorescence and Cherenkov light which is created by UHECR-induced EASs (see Fig. 2.1).

The mission concept was developed by the European Space Agency (ESA), the National Aeronautics and Space Administration (NASA), and the Japan Aerospace Exploration Agency (JAXA). It is the successor of the *Extreme Universe Space Observatory* (EUSO) mission concept of ESA, which was planned to be located on the

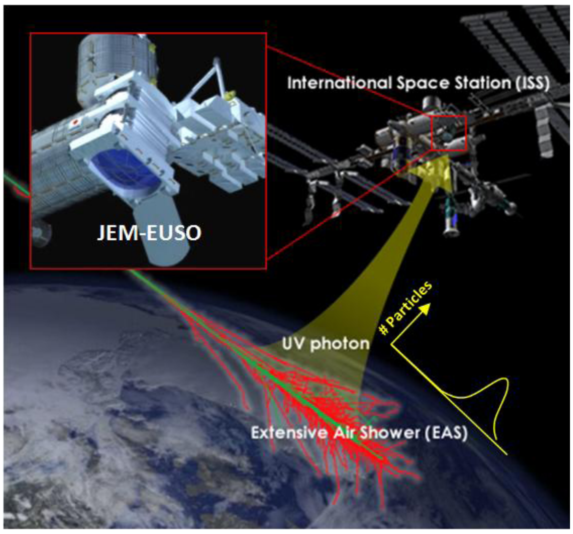

Figure 2.1: JEM-EUSO, designed to be mounted on the Japanese module on board of the ISS, is expected to detect CRs via the UV-light of EASs by looking down at Earth's atmosphere from space. (Image: JEM-EUSO Collaboration, 2010)

European module ‘Columbus’ of the International Space Station (ISS). Compared to EUSO, JEM-EUSO shall have an increased effective area, a decreased energy threshold, and shall be located on the Japanese Experiment Module (JEM) which is attached to ‘Kibō’ – the Japanese module of the ISS.[1]

Today’s UHECR-experiments are facing the challenges arising from the very low flux of the primary particles, resulting in the need for huge detector areas and long run-times to counteract the low statistics. Thus, fundamental questions like the origin and composition of the UHECRs could still not be solved up-to-date with the existing experiments – which even deliver partially contradicting results. JEM-EUSO will face these challenges with its unique observational approach: in contrast to the largest UHECR-experiments like the Pierre Auger Observatory (PAO)[2] and Telescope-Array (TA)[3], JEM-EUSO is not bound to a specific location on Earth. This approach has two big advantages compared to present experiments: first, a much larger effective area of about $1.4 \times 10^5\,\mathrm{km}^2$ at an orbit of 400 km altitude (Adams et al., 2013) – compared to $\sim 3000\,\mathrm{km}^2$ of the PAO; and second, a (nearly) uniform full sky coverage which is not possible with a ground-based experiment.

To demonstrate the technological and observational feasibility of this new detection method, several pathfinder missions have been designed. Among those are two balloon flights, which have already been executed successfully: the EUSO-Balloon and the EUSO-SPB. In addition, EUSO-TA, which is a ground-based telescope deployed at the TA site, is set-up using the prototype electronics developed for EUSO-Balloon and is used to test the EUSO observational technique, and further advance the electronics and the data-analysis software as well as to cross-calibrate the instruments with TA. For the two balloon missions, EUSO-TA and the Phase-A study of JEM-EUSO, hardware has been developed within the scope of this thesis.

The technology of these pathfinder missions and the flights of the balloons will be described in Chapter 3 and 4, while in this chapter, an overview of the JEM-EUSO mission is given.

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1 In the meantime, the acronym JEM-EUSO has been redefined to *Joint Experiment Missions for the Extreme Universe Space Observatory* by the collaboration. Nevertheless, JEM-EUSO refers to the original mission concept throughout this thesis.

2 The Pierre Auger Observatory is an international UHECRs experiment that is located in Argentina and observes the southern sky. It consists of several ground-based telescopes to detect the fluorescence light generated by the EASs as well as of an array of water-tank detectors, which measure the Cherenkov light that is created when a secondary particle of the EAS interacts with the water inside the tank. It is the largest experiment devoted to UHECRs and its 1660 surface detectors are distributed over an area of $3000\,\mathrm{km}^2$ (Abbasi et al., 2014).

3 The international Telescope-Array project is located in the desert of Utah and is monitoring the northern sky for UHECRs. It operates several fluorescence telescopes and an array of plastic scintillation detectors, which form a grid array of $\sim 700\,\mathrm{km}^2$ (Abu-Zayyad et al., 2012).

2.1 Scientific Objectives

As JEM-EUSO will increase the statistics for UHECRs with energies above 5.5×10^{19} eV by detecting 500 to 800 events per year (JEM-EUSO Collaboration, 2010), the mission will contribute to the answer of the basic questions of today's UHECR science, like

- the composition of UHECRs (see Section 1.2.1),
- the production process of such high-energetic particles (see Section 1.2.2),
- their origin and propagation (see Section 1.2.3), and
- a possible anisotropy in their flux (see Section 1.2.4).

In addition to these main objectives of the mission – as JEM-EUSO is a very fast and sensitive UV-telescope – it will also provide new insights into other topics of research, like:

- meteors, through the light that is emitted when they interact with the atmosphere;
- Transient Luminous Events (TLEs) which are different types of discharges in the atmosphere at an altitude of up to 100 km that may occur during thunderstorms;
- nightglow or airglow, i.e., faint light emitted in the upper atmosphere due to the formation of molecules like NO or OH at altitudes between 85 km to 300 km;
- extreme-energy γ-rays, which are also creating EASs, but with different characteristics than those created by UHECRs (i.e., no hadronic component): the shower maximum lies much higher in the atmosphere, and the EAS is more elongated. During the JEM-EUSO mission, the detection of > 3000 γ-rays with an energy $> 5 \times 10^{19}$ eV is expected (for more details, see Supanitsky et al., 2011);
- extreme-energy neutrinos, which have such a low cross-section with the particles of the atmosphere that neutrino-induced EASs are created at low altitudes or even through the interaction with Earth's crust, which leads to upwards-going EASs (see Bittermann (2010) for more information); and
- the Galactic magnetic field, through its interaction with CRs.

The science requirements as quoted from JEM-EUSO Collaboration (2010) are the following:

[SR1] 'Specification of UHECR origin by arrival direction analysis with determination accuracy better than a few degrees'

[SR2] 'Determination of trans-GZK structure in cosmic ray energy spectrum'

[SR3] 'UHECR primary identification capability: discriminating among nucleus, gamma ray and neutrino'

[SR4] 'Observation capability of Transient Luminous Events (TLEs)'

It should be noted, that these requirements are rather general and will hold for any future mission, devoted to the scientific investigation of UHECRs.

2.2 Observation Principle

The scientific objectives of JEM-EUSO will be obtained by deploying a UV-telescope in space, which monitors the Earth's atmosphere with a fast (400 000 frames/second) and sensitive (single photons) camera as depicted in Fig. 2.1. While the EAS evolves, a thin disk of secondary particles – the shower front – develops and is observable as a moving spot of UV-light, because of the generated fluorescence light. This spot becomes brighter until the EAS reaches its maximum and then fades out again. Due to the extreme energy of the primary particle, the shower front travels faster than the speed of light in the atmosphere and therefore additionally produces Cherenkov light, which also lies in the UV range and can be detected with the same instrument of JEM-EUSO (see Section 1.3 for more information about the detection of UHECRs).

Compared to EUSO, JEM-EUSO will have a lower energy-threshold of the primary particle of less than 5.5×10^{19} eV, which is realized by a higher quantum efficiency of the detector as well as improved trigger algorithms. A further increase of the effective area can be obtained when observing in the 'tilted mode', in which the telescope is tilted at an angle of 30° (from nadir), through which a larger section of the atmosphere can be observed. This leads to an increase of the effective area by a factor of 2.4: from $1.2 \times 10^5\,\mathrm{km}^2$ to $2.9 \times 10^5\,\mathrm{km}^2$, assuming an altitude of the ISS of 350 km (Shinozaki, 2010). The required accuracy for the determination of the arriving angle of the particles is obtained by the high timing (2.5 µs) and spatial resolution (0.074°, i.e., 510 m on ground) of the detector. More observational details about the experiment can be found in Table 2.1.

2.3 Technical Overview of JEM-EUSO

The main instrument of JEM-EUSO is a wide Field-of-View (FoV) telescope with a fast camera, sensitive to the fluorescence and Cherenkov light created by the EASs in

Table 2.1: Main parameters and requirements of the JEM-EUSO telescope (Adams et al., 2013; Bertaina et al., 2014; JEM-EUSO Collaboration, 2010).

Optical aperture	$4.5\,\mathrm{m}^2$
Field-of-View	64° (major axis) 45° (minor axis)
Observational area at $H_{orbit} = 400\,\mathrm{km}$	$1.4 \times 10^5\,\mathrm{km}^2$
Observed energy band	300 nm to 430 nm
Timing resolution	2.5 µs
Spatial angular resolution	0.074°
Pixel size at ground at $H_{orbit} = 400\,\mathrm{km}$	510 m (at the center) 610 m (at the edge)
Number of pixels	3.2×10^5
Energy threshold for primary particle	$\leq 5.5 \times 10^{19}\,\mathrm{eV}$
Energy determination accuracy at 60° zenith angle	$\leq 30\,\%$ for $E = 10^{20}\,\mathrm{eV}$
Arrival direction determination accuracy at 60° zenith angle	$\leq 2.5°$ for $E = 10^{20}\,\mathrm{eV}$

the UV bandwidth between 300 nm to 430 nm. In addition, it is equipped with an Atmospheric Monitoring System (AMS), which is required to monitor the atmospheric conditions, and is important for the correct reconstruction of the EASs. The AMS consists of an InfraRed (IR)-camera and a LIght Detection And Ranging (LIDAR)-unit. While the IR-camera can be regarded as an independent instrument, the main telescope will also function as the detector for the LIDAR.

In this Chapter, the main instrument of JEM-EUSO shall be discussed in more detail, since the hardware developed in the scope of this work is part of the read-out electronics of the main detector. In addition, the pathfinder projects – especially given their role as technology demonstrators – are heavily based on the main instrument of JEM-EUSO and its key technologies. The optics, the detector, and the read-out electronics of this UV-telescope, together with the working principles of the trigger algorithms will be described in the following sections. More information on the development of the L1 and L2 trigger algorithm, the prototype of the Cluster Control Board (CCB) and the hardware for the pathfinder projects can be found in Chapter 5 and in Bayer, 2011; Bayer et al., 2011, 2013.

2.3.1 Optics Module

The exact parameters of the instrument and especially of the Optics Module (OM) of JEM-EUSO is strongly driven by the available launcher and its size and mass constraints. The latest design meets the constraints of the Dragon launcher of SpaceX instead of the H-II Transfer Vehicle (HTV) from JAXA as it was originally planned. Nevertheless, the different designs share the same basic configuration, which consists of three lenses made out of PolyMethylMethAcrylate (PMMA): two curved double-sided Fresnel lenses, which are used as front- and rear-lens, are accompanied by an intermediate curved precision Fresnel lens in-between them. The middle-lens is added to correct for chromatic aberration effects and, therefore, to reduce the Point Spread Function (PSF). A schematic overview of the instrument with the position of the lenses is given in Fig. 2.2. To fit inside the unmanned transport vehicle that will lift JEM-EUSO to the ISS, the OM is equipped with extendable masts which will deploy JEM-EUSO to its full size of ∼ 4 m after it has been attached to the ISS. Any displacements of the lenses which might possibly be present after the deployment will be corrected by dedicated mechanics. For the HTV design, although the full diameter of the lenses is 2.65 m, two sides have to be cut down to 1.9 m. The entrance pupil together with the focal length of 2.3 m results in an F-number of 1. The entire mass of the lenses is ∼ 150 kg, and a spot size of 2.5 mm (RMS) can be achieved (Adams et al., 2015f). The resulting focal surface, which has a diameter of 2.2 m and on which the detector is located, possesses a spherical curvature of 2.505 m.

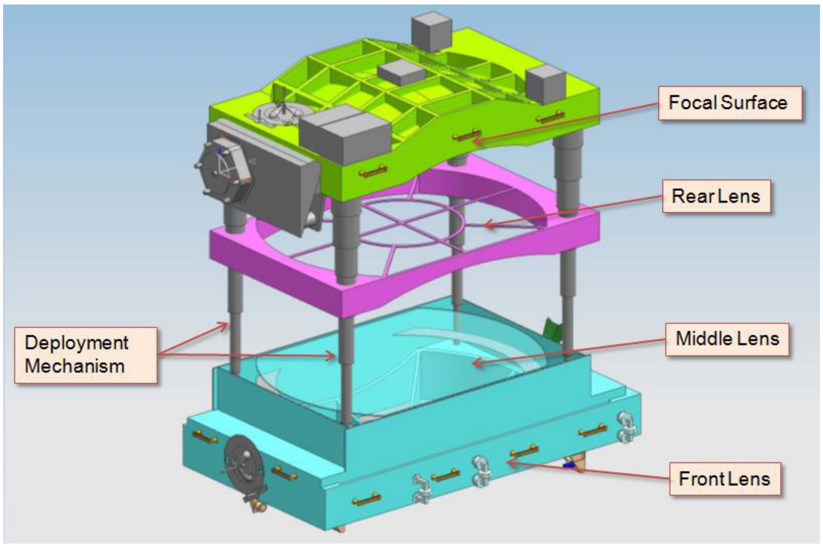

Figure 2.2: Schematic overview of the position of the front-, middle- and rear-lens of JEM-EUSO with respect to the detector, which is located on the focal surface. Also depicted is the deployment mechanism. (Image: JEM-EUSO Collaboration, 2010)

2.3.2 Focal Surface Detector

On the focal surface of the telescope, the UV-detector is located, which is designed in a modular structure (see also Fig. 2.3):

- the entire Focal Surface (FS)-detector consists of 137 Photo-Detector Modules (PDMs);
- each PDM consists of 9 Elementary Cells (ECs);
- each EC is composed of 4 Multi Anode PhotoMultiplier Tubes (MAPMTs); and
- each MAPMT has 8 × 8 pixels.

Thus, the entire FS-detector consists of nearly 5000 MAPMTs, resulting in more than 315 000 pixels. To be able to measure the space-time development of an EAS, the detector has a fast response time of 2.5 µs and a pixel FoV of $\leq 0.1°$. It is sensitive to single photons in the wavelength range of 330 nm to 400 nm (JEM-EUSO Collaboration, 2010).

The MAPMTs (see Figure 2.4) have been developed by RIKEN[4] in collaboration with Hamamatsu Photonics. Each MAPMT consists of 64 channels, which are arranged in an 8 × 8 array. Each pixel has a size of 2.88 mm × 2.88 mm, which leads to a sensitive area of max. 23.04 mm × 23.04 mm. The physical dimensions of each MAPMT are 26.2 mm × 26.2 mm × 17.4 mm (without the soldering pins). This smallest detector element has a quantum efficiency of around 35 % to 40 % in the wavelength range from 330 nm to 400 nm, and can be operated at temperatures from −10 °C to +30 °C (JEM-EUSO Collaboration, 2010). An overview of the parameters is given in Table 3.1. Every MAPMT is equipped with a UV filter, whose sides are cut in a trapezoidal shape which acts as a kind of 'Winston cone' and reduces the dead area between the MAPMTs.

2.3.3 Focal Surface Electronics

The main part of the electronics is located directly behind the FS-detector. This allows the hierarchical and parallel design already mentioned in Section 2.3.2, which simplifies the development and the integration phase, and improves the reliability with its intrinsic redundancy. At the same time, this concept puts strict and challenging requirements on the electronics – especially on size, mass, and power consumption – as they have to fit inside the detector envelope. The main duties of the electronics can be summarized into the following three tasks:

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[4] RIKEN is a natural sciences research institute in Japan.

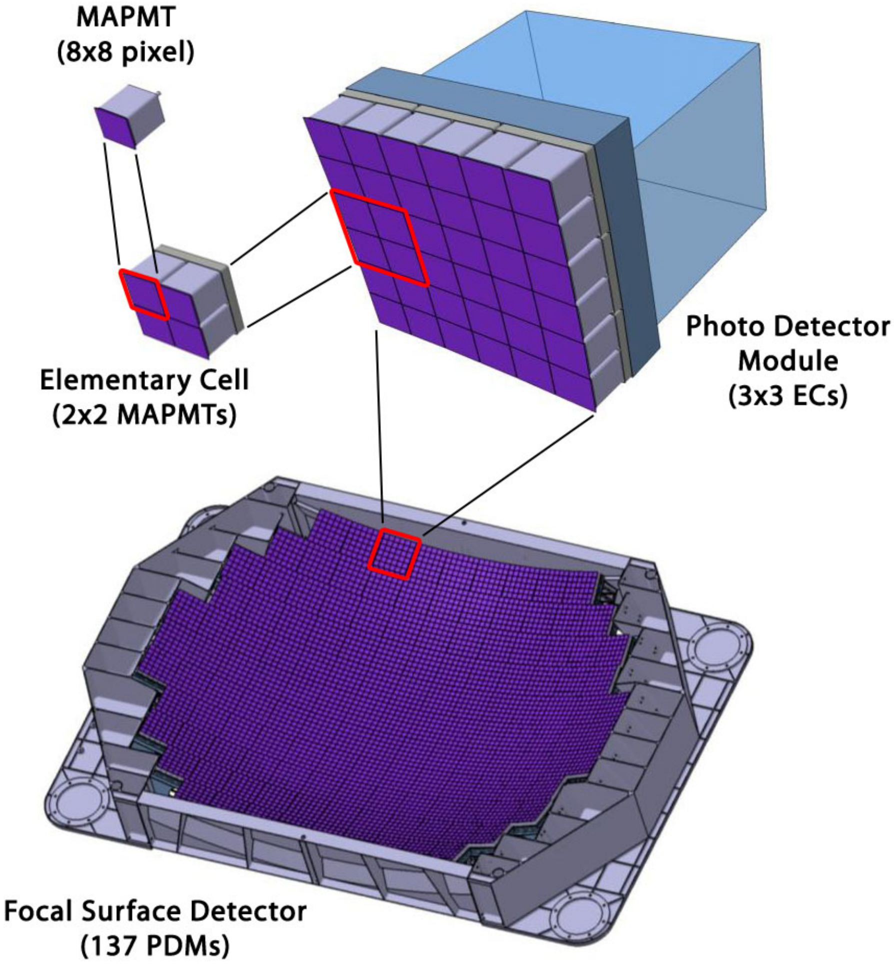

Figure 2.3: The UV-detector is designed in a modular structure. In total, it consists of more than 315 000 pixels which are organized in PDMs, which is the basic detector unit. (Image based on: JEM-EUSO Collaboration, 2010)

1. read out the detector and provide the analog-to-digital conversion;
2. reduce and store the scientific data, and make them available for the downlink to ground;
3. control and monitor the status of the whole system.

These tasks will be handled by various dedicated modules of which two have been developed or redesigned in the scope of this work – the Cluster Control Board (CCB) and the Photo-Detector Module (PDM) control board. The following sections will briefly describe the main functionalities of the different modules and give an overview of the data-flow of the instrument.

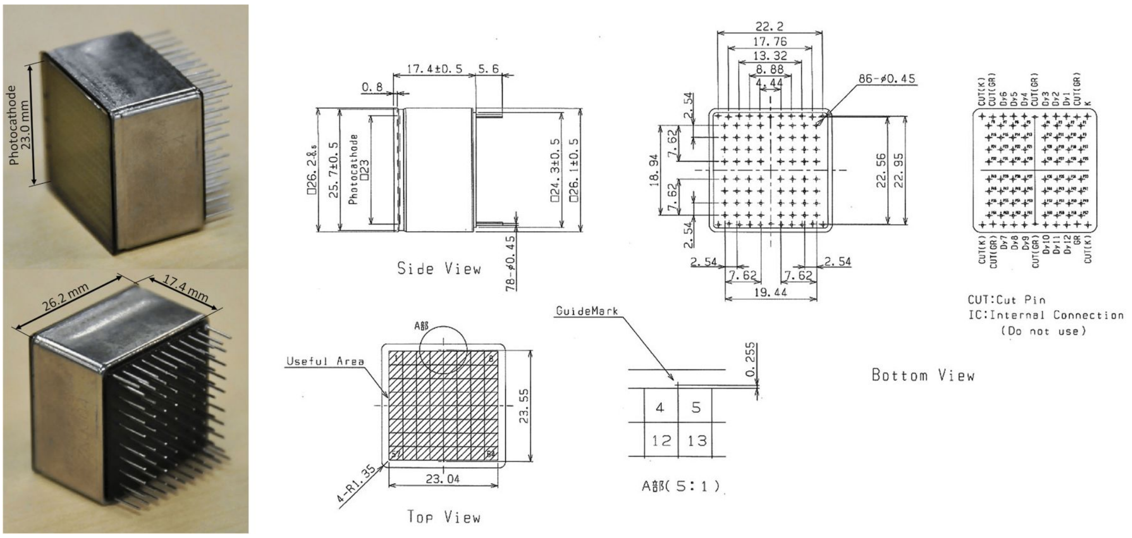

Figure 2.4: Images of the front- and backside of an MAPMT – the 'R11265-113-M64 MOD2' from Hamamatsu. (Image: Adams et al., 2015f)

In addition, other control and management systems are needed to operate the instrument: the management of the AMS, a thermal control system including sensors and heaters, calibration devices and the management of the lid mechanism. Details on these systems can be found in Adams et al., 2015a,c,e,f; JEM-EUSO Collaboration, 2010.

2.3.3.1 Front-End Electronics

A photon produced by an EAS inside the atmosphere eventually reaches the MAPMT and is converted to photoelectrons by the photocathode. These electrons are then multiplied with the help of a High Voltage (HV), which is applied to the dynodes (12 stages in total). The typically reached gain is of the order of 10^6 with 0.9 kV between the photocathode and the anode. Finally, the large amount of produced electrons results in a short current pulse at the anode and can be measured.

This measurement and the following analog-to-digital conversion is handled by an Application Specific Integrated Circuit (ASIC) which was specifically developed for the project – the Spatial Photomultiplier Array Counting and Integrating Read-Out Chip (SPACIROC). The ASIC has two modes implemented which are working in parallel: a 'single photon counting' mode, and a 'charge-to-time conversion' mode. These two modes are needed to handle the huge dynamic range imposed by the scientific requirements – e.g., neutrino induced showers are faint and short (a few nanoseconds) in contrast to the slow but very bright TLEs which can last for several hundred milliseconds.

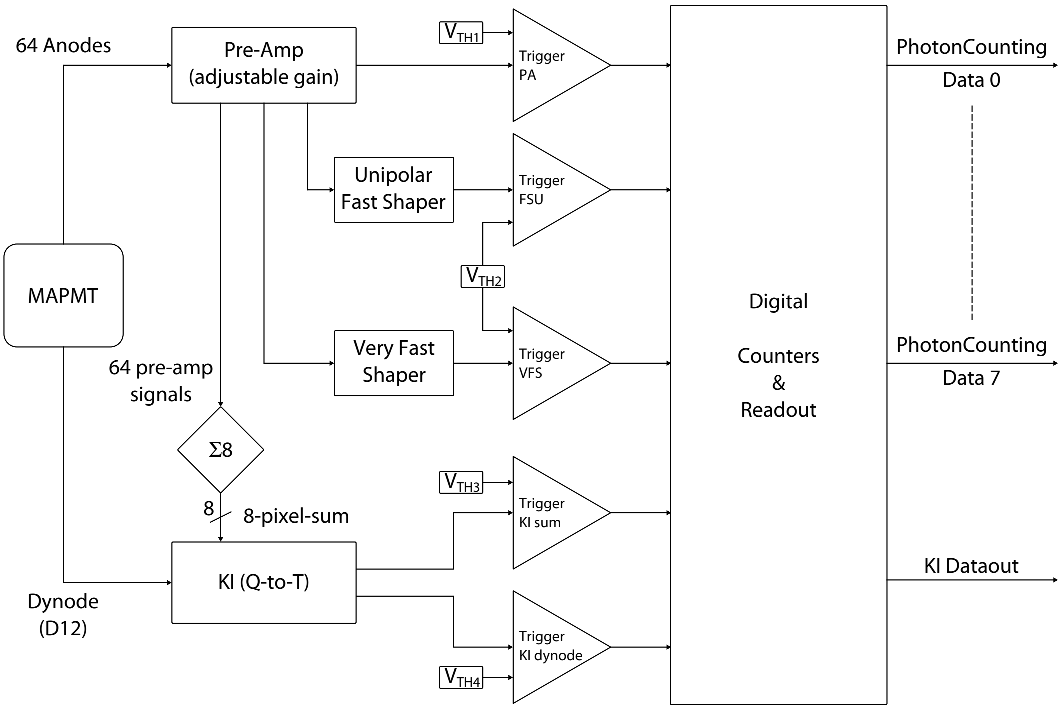

Figure 2.5: Block diagram of the SPACIROC: The 64 channels from one MAPMT are pre-amplified and shaped. For each channel, an adjustable trigger generates a fast digital signal, which is fed to a counter to count the single-photoelectron pulses during one GTU ('photon counting' part). An additional charge-to-time converter is fed by the signals generated from the sum of 8 channels ('KI') and by the signal from the last dynode (9 in total). This is done to increase the dynamic range in case of a bright source (e.g., lightning) and to protect the MAPMTs in case of too much light. (Image based on: Ahmad et al., 2010b)

Each ASIC will handle the signals coming from one MAPMT, as it can bee seen in Figure 2.5. Before the pulses from each of the 64 anodes can be counted in the digital part of the ASIC, the signal is pre-amplified, shaped, and discriminated in several stages. This signal conditioning is also the very first trigger stage, with the main purpose to reduce the electronic noise. Each charge-to-time integration module (nine in total) is fed with the sum of 8 pixels (because the imaging of very extensive phenomena does not require a high spatial resolution) and the signal coming from the last dynode. The signal of the last dynode basically gives access to the integrated signal of the whole photocathode, i.e., all 64 channels, and will therefore be used to generate a signal which will be used to protect the MAPMT in case of too much light.

Finally, the digital part of the SPACIROC counts the single-photoelectron pulses arriving during one Gate Time Unit (GTU), which is set to 2.5 µs, and provides an interface to access this information. A second digital interface is available to configure all the different parameters of the SPACIROC like the gains of the pre-amplifier or the thresholds for the photoelectron counting trigger. These ‘slow-control’ parameters have to be set each time the operation mode of the instrument changes. More details on the SPACIROC can be found in Ahmad et al., 2010a; Ahmad, 2012; Ahmad et al., 2012.

2.3.3.2 Photo-Detector Module Control Board

The entire PDM – which comprises 36 MAPMTs, their associated HV power supplies, 6 ASIC-boards (each equipped with 6 ASICs, respectively), the PDM control board, and the mechanical structure – forms the basic detector unit, and a total of 137 PDMs are arranged on the FS of the instrument.

The PDM control board, also referred to as PDM board, itself collects the digital data coming from 36 ASICs, continuously stores them inside a ring buffer which holds 128 GTUs, and evaluates the ‘L1’ trigger algorithm – also referred to as the Persistency Tracking Trigger (PTT) (see Section 2.4). This gives a total of 320 µs continuous data around each trigger (each of the 128 frames has 48 × 48 pixels with an exposure of 2.5 µs), which are sent to the CCB for further processing. In addition to this main task, the PDM control board also configures the baseline parameters of the SPACIROC and provides an interface to change these parameters during the operation of the instrument. More details on the PDM control board can be found in Jung, 2017, and technical details on its re-design and implementation, which were performed within the scope of this work, are given in Section 5.3.

2.3.3.3 Cluster Control Board

To further reduce the amount of data and suppress the background, another level in the hierarchy of the read-out electronics is introduced with the CCB. In case of an L1 trigger, this board receives or requests the data packets from a cluster of PDMs via a fast data interface (while the baseline cluster consists of 8 adjacent PDMs, the advanced option foresees a cluster of 9 PDMs). The main task of the CCB is the evaluation of the second level trigger (L2) – also called Linear Track Trigger (LTT), see Section 2.4 – and the buffering of the data until they can be sent to the Mission Data Processor (MDP) in case of a positive trigger. Due to the hierarchical structure of the instrument, the CCB also has to act as a relay and pass commands and configuration data to the connected PDMs and monitor their status. The hardware implementation and design of the prototype CCB is described in Section 5.1, and the development of a ‘scaled down’ version (interfacing only one PDM) for the pathfinder projects can be found in Section 5.2.

2.3.3.4 Mission Data Processor

The central MDP or just Data Processor (DP) controls the whole system and provides the command and data interface to the external world via the ISS (JEM) communication interface. As the downlink is not available all the time, the DP has to provide and manage the on-board storage and to buffer the data received from the connected CCBs. It also monitors the status of the system with the help of the Housekeeping (HK) system, which regularly collects engineering data and evaluates the overall health status of the instrument.

2.4 Trigger and Read-Out

To reduce the huge amount of data produced by the detector (more than 1 Tbit s^{-1}) to a data rate which is manageable by the downlink of the ISS (around 300 kbit s^{-1}) several trigger stages have been developed. Besides the analog signal discrimination, the two main trigger algorithms are implemented inside the PDM- and CCB-electronics. These two trigger algorithms are described in the following sections, while their hardware implementation can be found in Chapter 5.

As it can be seen from the estimated trigger rates given in Table 2.2, the very first trigger level (‘Counting trigger’), which is implemented as a simple threshold discrimination inside the analog part of the SPACIROC, already reduces the trigger rate by a factor of around 10^3 by rejecting electronic noise and filtering out the single-photoelectron pulses produced at the anodes of the MAPMTs. The following stage further reduces the trigger rate by a factor of 10^5 by only accepting signals with a specific duration or persistency, which is implemented in the PDM control board. Finally, the Linear Track Trigger (LTT) – implemented in the CCB – only accepts signals with a specific space-time development resulting in a trigger rate of

Table 2.2: The estimated trigger rates at the different trigger levels (JEM-EUSO Collaboration, 2010).

		Trigger rate at level of	
	Level	PDM	FS
	Photon trigger	9.2×10^8 Hz	1.4×10^{11} Hz
	Counting trigger	7.1×10^5 Hz	1.1×10^8 Hz
L1	Persistency trigger	7 Hz	1.0×10^3 Hz
L2	Linear Track Trigger	6.7×10^{-4} Hz	1.0×10^{-1} Hz
	Expected rate of CR events	6.7×10^{-6} Hz	1.0×10^{-3} Hz

around 0.1 Hz, which is manageable by the DP.

2.4.1 L1 Trigger Algorithm

The first level trigger – or Persistency Tracking Trigger (PTT) – algorithm accepts only signals above the mean background level, which are locally persistent for a few GTUs. Each MAPMT is independently partitioned into cells of 3×3 pixels which are overlapping each other by one pixel. This results in 36 cells per MAPMT which are evaluated independently and in parallel. Every time a pixel inside one cell is equal or above a threshold N, the following questions are evaluated:

1. Is there (inside the cell) any signal which is active (meaning equal or above the threshold N) for at least R GTUs during a slot of P consecutive GTUs?
2. Is the total of detected photoelectrons inside the cell above a threshold S?

It should be stressed that the first condition is fulfilled as long as any pixel inside the cell is active regardless of the exact position which is important because the light spot produced by the EAS is moving. In addition, R has to be smaller or equal than P, while $R < P$ basically means that the signal is allowed to vanish (smaller than N) and reappear again.

The values of R and P define the trigger mode and can be adjusted to suite the operating conditions of the instrument. This is necessary, because in case of the pathfinder missions, i.e., the balloon flights and the ground based telescope EUSO-TA, the instrument is much closer to the EAS (between 1 km to 30 km) than during the JEM-EUSO mission. Therefore, the most suitable values for EUSO-TA are $P = 0$ and $R = 0$, while for EUSO-Balloon and EUSO-SPB $P = 0$ and $R = 1$ or $P = 1$ and $R = 1$ is more suitable. In contrast, the distance to the EAS for JEM-EUSO is around 400 km and these parameters will be set to $P = 5$ and $R = 3$. These values were determined via simulations and confirmed during the field tests (see also Abdellaoui et al., 2017; Bertaina et al., 2015; Suino et al., 2015). The parameters N and S will be set according to the average background, and some additional logic is implemented which continuously evaluates the current background and automatically adjusts the thresholds to keep the trigger rate below the requirement of 7 Hz per PDM.

This logic cannot discriminate between the relatively short events generated by an EAS and the long lasting events from TLEs and meteors or even much slower signals generated by airplanes, ships, or cities. Therefore, an additional condition on the level of an EC is evaluated and needs to be fulfilled before an L1 trigger is issued to the CCB. Starting with the first GTU in which the first level trigger fires (on any of the four MAPMTs forming an EC), a simple counter is started, which is incremented each time a first level trigger fires again. After a preset number N_{GTU} of consecutive GTUs, the counter value is checked against a threshold N^{thr}_{GTU}. Finally, only if the counter value is below N^{thr}_{GTU}, a trigger is issued – or if the signal lasted longer than N^{thr}_{GTU}, the data are rejected. The current values for these parameters are $N^{thr}_{GTU} = 72$ and $N_{GTU} = 72$. This configuration basically rejects all events which last longer than 180 µs inside one EC – the maximum expected time during which an EAS event is visible inside one EC is less than 45 GTUs for JEM-EUSO.

In case of an L1 trigger, the information on the triggering cell(s) is made available and will be used as a seed to evaluate the L2 algorithm.

More details on the hardware implementation of the L1 trigger algorithm can be found in Section 5.3.1 and in Bayer et al., 2017.

2.4.2 L2 Trigger Algorithm

The L2 trigger algorithm – or Linear Track Trigger (LTT) – uses the geometrical properties of the temporal EAS development and its projection onto the FS to search for the specific signatures in the signals arriving at the instrument.

While an UHECR induced EAS develops, the shower front produces a thin luminous disc, which travels ultra-relativistically through the atmosphere (see also Section 1.3). The amount of produced light is increasing as long as the EAS evolves and new particles are generated, until the shower maximum is reached, after which it becomes fainter and finally vanishes. From a typical EAS, generated by a proton with an energy of 10^{20} eV, several thousand photons will be detected during a duration of tens to hundreds µs (Adams et al., 2015b). Due to the high spatial and timing resolution of the instrument, this luminous disc will appear as a small spot with the size of a few pixels which moves from frame to frame on a straight line. The incident angle of the incoming UHECR and, accordingly, the orientation of the shower axis will dictate the speed and direction of this (projected) movement and can be calculated as follows.

As the EAS propagates approximately with the speed of light c on a straight line, the light reaching the detector is delayed from the passing shower front by the time (see Figure 2.6)

$$\Delta t = \frac{\overline{AB} + \overline{BC}}{c}\,. \tag{2.1}$$

Or in other words: the time needed in order to see the light spot moving from point A to C (from the point of view of the detector) is equal to the time needed for the shower front to move from A to B plus the time needed by the photons to travel from B to C. By substituting with the following trigonometric relations

$$\sin\theta = \frac{\overline{AC}}{\overline{AB}}, \quad \tan\theta = \frac{\overline{AC}}{\overline{BC}}, \quad \tan\theta = \frac{\sin\theta}{\cos\theta}, \quad \text{and} \quad \tan\frac{\theta}{2} = \frac{\sin\theta}{1+\cos\theta},$$

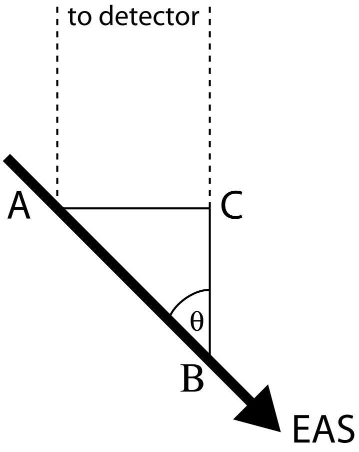

Figure 2.6: Schematic of an EAS that is inclined with respect to the detector surface.

it follows

$$\Delta t = \frac{\overline{AC}}{c \cdot \tan\frac{\theta}{2}} \,. \tag{2.2}$$

With the definition of Δx and Δy as the projections on the focal surface expressed in number of pixels and ΔL as the on ground pixel size, it results that

$$\overline{AC} = \Delta L \cdot \sqrt{\Delta x^2 + \Delta y^2} \tag{2.3}$$

and, finally,

$$\theta = 2 \arctan\left(\frac{\Delta L}{c \cdot \Delta t} \cdot \sqrt{\Delta x^2 + \Delta y^2}\right) \,. \tag{2.4}$$

For the azimuth angle ϕ of the EAS, it directly follows from trigonometry that

$$\phi = \arctan\left(\frac{\Delta y}{\Delta x}\right) \,. \tag{2.5}$$

The duration Δt – i.e., the exposure of the instrument – is set in a way that, for a horizontal shower ($\theta = 90°$), it equals the time Δt which it takes for the spot to cross one pixel, and is called GTU:

$$\Delta t = \frac{\Delta L}{c} \cdot \underbrace{\left(\frac{\sqrt{\Delta x^2 + \Delta y^2}}{\tan\frac{\theta}{2}}\right)}_{=1} \approx \frac{750\,\mathrm{m}}{3 \times 10^8\,\mathrm{m/s}} = 2.5\,\mu\mathrm{s} \,. \tag{2.6}$$

It should be stressed that this value is depending on the exact on-ground pixel size, and therefore not only on the instrument itself (optics and MAPMT), but also on the orbital height of the ISS, which is changing over time. As it can be seen from Equation (2.6), the 2.5 µs is based on an older design of the instrument which had an on-ground pixel size of 750 m and is larger than the one for the current design, which is 510 m (see Table 2.1). As the GTU has a big impact on the electronics and the data rate, it had to be fixed at some point to finalize the design of the ASIC and the electronics. Nevertheless, the length of the GTU may be subject to change.

The LTT intends to follow the development of the EAS and the resulting movement of the spot on the FS over some predefined time N_{GTU}^{L2}. By doing so, the algorithm can recognize the peculiar signature produced because of the ultra-relativistic development of the shower front. As the angles θ and ϕ of the incoming UHECR are obviously not known, a brute-force approach is chosen and a predefined set of directions is used which covers the whole parameter space ($\theta = 0° \dots 90°$ and $\phi = 0° \dots 360°$). Based on the location of the triggering cell from the L1 trigger, several 3×3 pixels boxes are defined around this trigger seed. By using the Formulas (2.4) and (2.5), the apparent movement on the FS is calculated and each box is 'moved' accordingly in Δx and Δy from frame to frame, and the detected counts inside the box are integrated. From these integrated values – one for each direction $(\theta_n|\phi_n)$ and box – the maximum value is compared to a threshold above the background, and eventually a trigger will be issued in case this threshold has been exceeded. The maximum of the integrated counts will be found in case the box (exactly) follows the spot, otherwise only background or parts of light from the shower will be integrated. This very coarse information on the shower axis could then be used for example by the LIDAR to measure the atmospheric conditions along the EAS.

The integration over the complete parameter space is a time consuming task, especially as the available computing power is limited due to the strong constraints for space qualified hardware regarding power consumption, weight, and size. Therefore, the number of single integrations must be tailored to suite the flight hardware without taking the risk of losing events because the selected parameter space was too coarse. This problem was evaluated in Bayer, 2011 and led to the current baseline configuration of the L2 algorithm. This implementation defines a total of 375 boxes, distributed over ±7 GTUs around the trigger seed, and a total of 67 different directions $(\theta|\phi)$. The integration in time for each box and direction is done for $N_{GTU}^{L2} = \pm 7$ GTUs.

The LTT algorithm has one important limitation, and it should be stressed that this drawback is inherent of how the algorithm works and not coming from the above mentioned limitations on the hardware. Due to the projection onto the detector, the spot of a horizontal shower moves one pixel per GTU, but a vertical shower will not move at all. Therefore, the algorithm cannot discriminate between a vertical shower and a steady or slowly moving light source as it works on a fixed and short timescale. To counteract this problem, additional logic was added to the L1 algorithm which basically filters out all events which are lasting too long (see Section 2.4.1).

More details on the hardware implementation of the L2 trigger algorithm can be found in Section 5.2.3 and in Bayer, 2011; Bayer et al., 2011, 2013.

3 EUSO-Balloon

Ever since the beginning of the 20th century, when Victor Hess, Alfred Gockel, and Karl Bergwitz conducted their experiments, CRs and balloon flights are deeply connected. While the available technology developed immensely during the last 100 years, the basic concept and even the basic detector technology of the balloon flights remained the same: detecting CRs by observing their interaction with Earth's atmosphere. But in contrast to the early balloon experiments, which detected the CRs via the charged secondary particles produced in the EAS, the observational principle of EUSO-Balloon is to detect the fluorescence light produced by the secondary charged particles and, from that, deduce the properties of the primary CRs.

EUSO-Balloon is one of several pathfinder projects which were defined within the JEM-EUSO collaboration and have the main objective to advance and demonstrate the technology planned for JEM-EUSO: a small version of the JEM-EUSO detector – one complete PDM (see Section 2.3.2 and Figure 2.3) – is deployed at the TA site (named EUSO-TA) under the leadership of the Japanese collaborators, and another two PDMs were brought to near-space on-board stratospheric balloons, namely EUSO-Balloon and EUSO-SPB. EUSO-Balloon was built in collaboration with the Centre National d'Études Spatiales (CNES) – the French Space Agency – together with the Canadian Space Agency (CSA), who provided the infrastructure at the launch site. EUSO-SPB was developed in collaboration with NASA and launched by the Columbia Scientific Balloon Facility (CSBF).

In this chapter, the EUSO-Balloon project will be introduced, and important technical differences with respect to the EUSO-TA hardware will be highlighted.

3.1 Project Schedule

Precisely 100 years after Hess (1911) and Gockel (1911) performed their first successful balloon flights in 1911 – which led to the detection of CRs – the EUSO-Balloon project was officially started with the 'Kick-Off Meeting' in September 2011. Already at the end of the same year, the feasibility of the experiment was demonstrated and the Phase-A study came to its successful conclusion. Seamlessly following, the instrument definition phase – or Phase-B – was carried out, and in parallel, several crucial subsystems with long lead-times were already procured and produced, like the MAPMTs or the lenses. In addition, the first prototypes of several subsystems were produced and first tests performed. With the beginning of the Phase-C/D in early 2013, all the subsystems were manufactured and tested, and finally, the flight model of the instrument was integrated and tested. This last phase concluded with the 'Flight Readiness Review' at the beginning of June 2014 and the shipment of the instrument to Timmins, Canada.

Eventually, not even three years after the 'Kick-Off Meeting', the EUSO-Balloon project successfully accomplished its flight. It was launched on August 25th, 2014 at 0:53 Coordinated Universal Time (UTC), from the Stratospheric Balloon Base in Timmins (Ontario, Canada) after one week of final flight preparations. A total flight time of 8 hours (including the ascent) allowed 5 hours of data taking, and the launch campaign was completed with the successful recovery of the instrument and its recorded data.

3.2 Objectives and Requirements

Designed as a proof of concept and test-bench for JEM-EUSO as well as for space-based CR experiments in general, the following objectives were defined for EUSO-Balloon together with their corresponding science (SR) and mission (MR) requirements (Ballmoos et al., 2013, 2012).

3.2.1 A-level: Technology Demonstrator

The highest priority (A-level) was dedicated to the end-to-end test of the key elements of the JEM-EUSO detector. This does not only include the various elements of the front-end electronics like the MAPMTs and the ASICs, but also covers the different hard- and software algorithms needed for the triggering on CR events. In addition, the balloon flight was aimed at raising the Technology Readiness Level (TRL) of various JEM-EUSO parts. The requirements are stated in Ballmoos et al., 2012 as follows:

[SRA1] 'A payload representative of JEM-EUSO shall be made to work at a float level above 40 km and take data in low background conditions, as well as in intense background conditions caused by artificial background.'

[SRA2] 'After each flight, the payload shall be recovered for further tests/flights.'

[MRA1] 'Accommodate a payload representative of the basic JEM-EUSO acquisition module (PDM + CCB) and which includes an optical system. Also, all HV (switch) systems must be able to work in vacuum, i.e., at a 3 mbar float level.'

[MRA2] 'Flight data recording at float level over land is expected to last at least 3 hours during a moonless part of the flight, and 3 hours during a moonlit phase ($< 25\,\%$ full).'

[MRA3] 'Flight data at float level shall include sudden background enhancements due to city lights etc.'

[MRA4] 'The instrument must be built as to withstand landing and (late) recovery at sea, or a landing with 1 parachute out of 3.'

3.2.2 B-level: Real Data & Background

The B-level objective was dedicated to obtaining real data on the UV background of the Earth's atmosphere, with a spatial and timing resolution comparable to the one of JEM-EUSO. In particular, the same timing resolution of $2.5\,\mu s$ was implemented, but with a higher on-ground spatial resolution of 166 m (assuming a float altitude of 38 km and a FoV of ±6°). The smaller on-ground pixel size compared to JEM-EUSO was mainly constrained by the fixed pixel size of the MAPMTs and by limitations in the manufacturing process of the lenses, which in turn determine the FoV.

It should be obvious that the background is constantly changing as the environmental conditions are changing. This includes, for example, large-scale effects like moon phases or the nightglow, as well as on small scales towns or thunderstorms. In addition, the amount of reflected light (both background light and the back-scattered Cherenkov light) is highly dependent on the ground surface properties or on the presence of clouds. To adjust and fine-tune the trigger algorithms, it is therefore essential to acquire real background data under varying conditions (e.g., over different ground surfaces like forest or water and with different cloud coverages). The B-level requirements are listed in Ballmoos et al., 2012 as follows:

[SRB1] 'Acquisition of JEM-EUSO-type data, test the trigger algorithm performances. Priorities for collecting data are in descending order:

  [SRB1a] over ocean (moonless)
  [SRB1b] over ocean (moon)
  [SRB1c] over land (moonless)
  [SRB1d] over land (moon)

Each pixel of the PDM will be calibrated absolutely in efficiency with a precision better than $2\,\%$. The gain of pixels will be adjusted within $1\,\%$. We therefore want to experimentally confirm the effective background below 40 km, perform the acquisition of JEM-EUSO-type data, and adjust the trigger algorithms with real data.'

[SRB2] ‘Operation of an IR camera to measure temperature/altitude of cloud cover.’

[MRB1] ‘A second balloon flight shall fill in the B-level requirements [SRB1] that were not achieved in a first flight. Since the first priority is [SRB1a] - the launch site/season will be chosen to allow for a flight over an ocean, the precise launch date shall allow to observe at least 2 h at a float level of 3 mbar.’

[MRB2] ‘Testing the operation of a prototype IR camera on the EUSO-Balloon gondola.’

3.2.3 C-level: Precursor Mission

Based on the very low flux of UHECRs and the small size of the telescope, an estimation on the detectable UHECR events gave 0.2 to 0.3 events per 10 h of observation with a CR energy greater than 2.1×10^{18} eV (Ballmoos et al., 2013). Therefore, the detection of a ‘real’ event was regarded as negligible and treated as C-level objective.

As an advanced option, laser-induced events have been generated inside the FoV of the telescope. For this purpose, a helicopter was equipped with a laser, a Xenon flasher, and an UV-Light-Emitting Diode (LED) to generate various light signatures on which the electronics could trigger (see also Eser et al., 2015 and Adams et al., 2015g for more details). The C-level requirements as given by Ballmoos et al., 2012 are:

[SRC1] ‘Detection of several (≥ 10) representative CR events.’

[MRC1] ‘Long-duration-flight operation (≥ 50 h at night, To Be Confirmed (TBC)) of the EUSO-Balloon instrument in trigger mode and in low background configuration. Altitude loss down to 35 km (TBC) is acceptable after 3 day/night transitions.’

[MRC2] ‘Measure temperature/altitude of cloud cover with the IR camera.’

[MRC3] ‘Fly a co-aligned laser on the gondola; generate laser induced events during tagged data acquisition.’

[MRC4] ‘Choose launch date to allow for a part of the flight over a high reflectivity surface (clouds, snow ...).’

3.3 Technical Aspects of EUSO-Balloon

For EUSO-Balloon, a 400z Zodiac balloon was used with a maximum volume of 400 000 m^3, which leads to an envelope length of $\sim 140\,\mathrm{m}$ during launch and $\sim 90\,\mathrm{m}$ in diameter at float altitude. The structure of the pressure-less stratospheric balloon used for EUSO-Balloon and the various parts of the flight train are shown in Figure 3.1. Because of the operating principle of a zero-pressure balloon, where – in contrast to super-pressure balloons (see Section 4.2) – the pressure inside the balloon is always equal to the pressure outside, the float altitude of around 40 km is reached as soon as the Helium fills the complete volume of the balloon envelope. At this point, helium can escape at the bottom of the balloon and the ascent will be stopped. To counteract the changes in altitude between night and day, which are caused by the change in temperature and the resulting change in the volume of the balloon, the altitude can be controlled by releasing ballast in form of small steel bullets. To safely terminate the flight, helium can be released through a valve (see (1) in Figure 3.1) which is located at the top of the envelope. Directly attached to the envelope follows the Nacelle EnVeloppe (NEV) or the 'envelope gondola' (3), which accommodates a Global Positioning System (GPS) receiver and a transponder, allowing to track and recover the envelope after its separation from the payload for the descent.

The second part of the flight train is attached via a remote controlled separator (4) to a parachute (5) which will slow down the payload during descent, thus enabling a safe landing of the payload on ground. One requirement for the hardware is to withstand a shock of 10 g, which is the maximum acceleration when the parachute opens after separation from the balloon envelope. Following the parachute, the next element in the flight train is the Nacelle de Servitude Opérationnelle (NSO) or 'avionics gondola' (6), which contains all the flight control computers, the avionics, an aviation transponder, and the ballast. The NSO, together with the 'S band[1] antenna gondola' (7), is also responsible for establishing the radio link between the flight hardware and the ground segment. For safety reasons, an additional 'beacon light gondola' (8) is present, which ensures the visibility of the flight train during night and is especially needed during ascent and descent. Last but not least, the 'scientific gondola' (9) completes the flight train. This payload is described in more detail in the following sections.

3.3.1 Overview of the EUSO-Balloon Gondola

A schematic drawing of the scientific gondola is given in Figure 3.2. It can be divided into two main parts: the optical bench – i.e., the telescope – which supports the three

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[1] The S band is a frequency band that lies within the microwave regime, ranging from $\sim 2\,\mathrm{GHz}$ to 4 GHz.

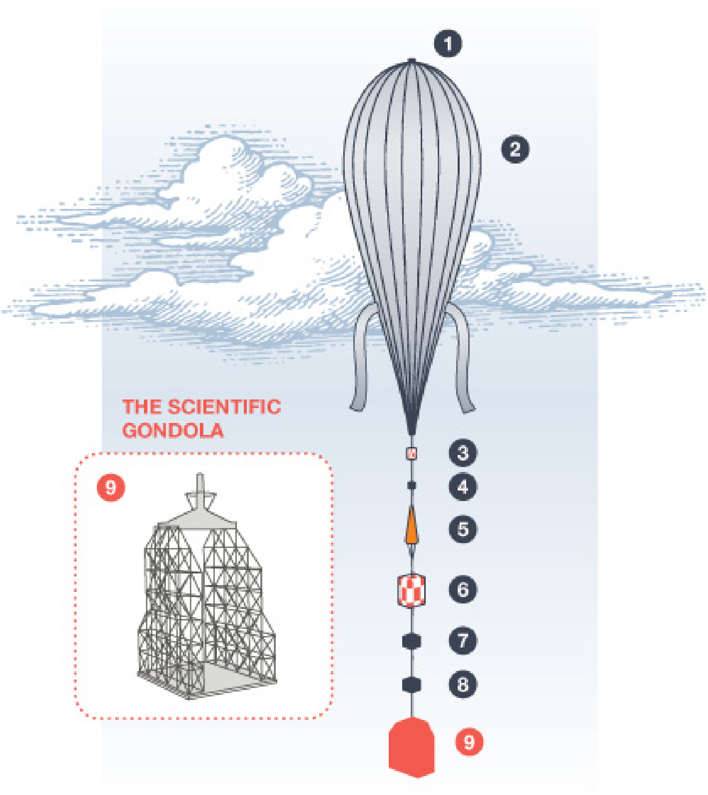

Figure 3.1: Schematic drawing of the various elements constituting the flight train of EUSO-Balloon, including the scientific gondola (highlighted in red). (Credit: Canadian Space Agency)

lenses (see Section 3.3.2), and the instrument booth which contains the electronics (see Section 3.3.3). Due to the mission requirement of a sea recovery (see [MRA4] in Section 3.2.1), several features were developed and implemented to protect the electronics in case of a splash-down:

1. Calibrated holes in the optical bench help to decelerate the gondola by releasing the enclosed air in a controlled manner. This avoids a submersion of the instrument booth.

2. A floater mounted at the top of the gondola and around the instrument booth keeps the instrument afloat.

3. The instrument booth was designed to be watertight, which was achieved by using the third lens to form a sealed compartment for the electronics.

4. In case of small water ingress (because of a damage or late recovery), the electronics were mounted above the waterline.

The dimensions of the flight-ready instrument are 2.58 m × 2.58 m × 3.70 m which includes the floater and the crash pads, which are mounted at the bottom of the gondola. As the structure of the gondola is made out of 'Fibrelam' aerospace panels which have a laminated honeycomb structure, the overall launch mass was only 467 kg.

The FoV of the telescope is 11° × 11°, which leads to an on-ground pixel size of 150 m. This is a compromise between manufacturing constraints and the A-level requirement to build a representative JEM-EUSO instrument, which would mean an on-ground pixel size of around 510 m. The UV light (290 nm to 430 nm) which reaches the telescope's entrance window from the bottom is focused onto the PDM, which is the basic detector unit of JEM-EUSO (see Section 2.3.2 and Figure 2.3). The signal from the MAPMTs is then digitized by ASICs, analyzed by the Field Programmable Gate Arrays (FPGAs) on the PDM control board and the CCB, and finally either stored on Solid State Drives (SSDs) by the DP or sent to ground via radio transmission (see also Section 2.2ff.).

To complete the instrument, an IR camera was mounted piggyback at the bottom of the telescope to be able to reconstruct the cloud height during the flight. The IR camera was a completely autonomous module sharing nothing more than a mechanical interface with the rest of the instrument. For that reason, the camera was mounted in a pressurized box[2] – thus, water-tight by design – together with a Central Processing Unit (CPU), mass memory in form of an SSD, auxiliary electronics, and a battery pack. More details on the IR camera can be found in Rodriguez Frias et al., 2015.

During the final integration of the instrument in Toulouse and Timmins, a few more independent instruments were added to the main gondola:

Optical Camera A small camera, sensitive to optical and also slightly to IR light, was added to help with the geo-referencing of the scientific data. Since the gondola was not stabilized and therefore spinning[3] during the flight (possibly with a small tilt), geo-referencing is nontrivial, and any additional information was regarded as useful. The camera was set to take pictures at a rate of 0.2 Hz with a resolution of 3680 × 2760 pixels. Unfortunately, the battery could not deliver enough power for the complete flight, and therefore, only data from the first three hours of the flight are available (until 4:03 UTC).

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[2] The IR camera housing was filled with 1 bar of dry nitrogen to simplify the thermal design and to avoid condensation on the entrance window.

[3] The complete flight train can be regarded as a large torsion pendulum. The frequency of the oscillation during the flight was ~ 6.5 mHz (Abdellaoui et al., 2019).

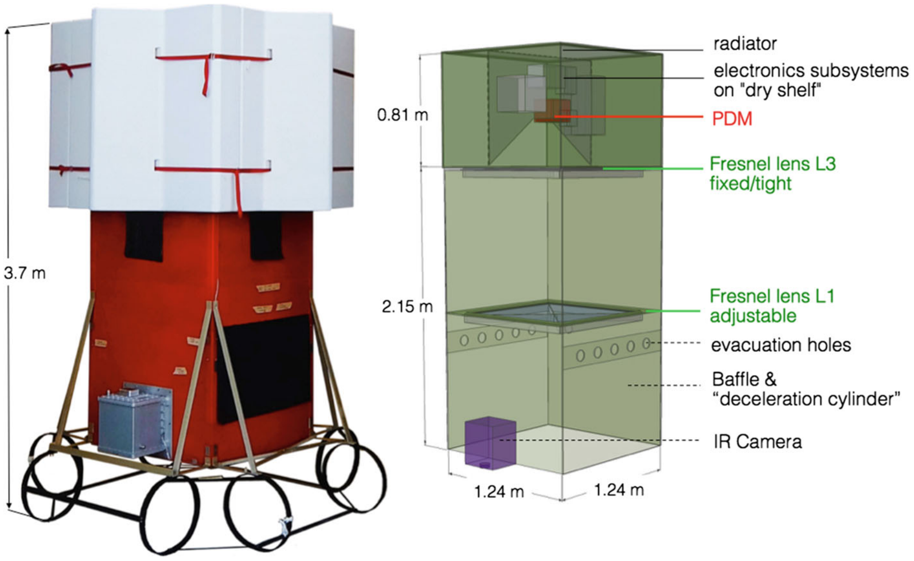

Figure 3.2: Picture of the EUSO-Balloon scientific gondola in flight configuration (left), and a schematic drawing of the final instrument (right). (Image: Adams et al., 2015d)

Radiation Monitor A handheld-sized Geiger-Müller counter[4] was put into an additional box on the top of the gondola to monitor the radiation environment. The data (in units of counts per second) were sent every 5 s via Universal Serial Bus (USB) to a smartphone which stored the data during the flight. The energy thresholds of the detector are given in S.E. International, Inc, 2014 as:

- minimum α-energy: 2 MeV
- minimum β-energy: 0.16 MeV
- minimum γ-energy: 10 keV

Photodiode A calibrated photodiode sensor[5] was mounted on the focal surface beneath the MAPMTs of the PDM. The sensor was connected to an energy- and power-measurement device which was located in the same box as the radiation monitor. This sensor was mainly used during the integration and the final tests on the launchpad as a safety check before switching on the HV of the MAPMTs. By reading out the current measurement, it was ensured that the light level was low enough not to damage the MAPMTs. To enable this check, one side of the box was sealed with a transparent window.

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[4] Radiation Alert Inspector from S.E. International, Inc.

[5] PD300-UV from Ophir Optronics Solutions Ltd.

3.3.2 Telescope Subsystem

The optics of the telescope consisted of three lenses made out of PMMA – similar to JEM-EUSO, but on a smaller scale: the aperture is 1 m × 1 m. To comply with the schedule of EUSO-TA and EUSO-Balloon, the two projects share the same front- and rear-lens design. Since the requirement on the Root Mean Square (RMS) spot size of the EUSO-TA optics is less strict[6] (smaller than the size of an MAPMT) than for EUSO-Balloon (smaller than the pixel size), a third lens was only added to EUSO-Balloon to correct for chromatic aberration – as for JEM-EUSO. A side-by-side comparison of the two designs and their resulting spot sizes for different incident angles is given in Figure 3.3.

The front- (L1) and rear-lens (L3) are aspherical flat Fresnel lenses with focal lengths of 2585.6 mm and 600.2 mm, while the middle-lens (L2) is a diffractive lens with a focal length of 3856.9 mm.[7] Each lens is 8 mm thick, which leads to a mass of 9.6 kg each. Since the lenses are quite heavy and thin at the same time, a mechanical support structure – the 'spider' – was added to reduce the bending of the lenses under their own weight. Because landing in water is possible for EUSO-Balloon (see

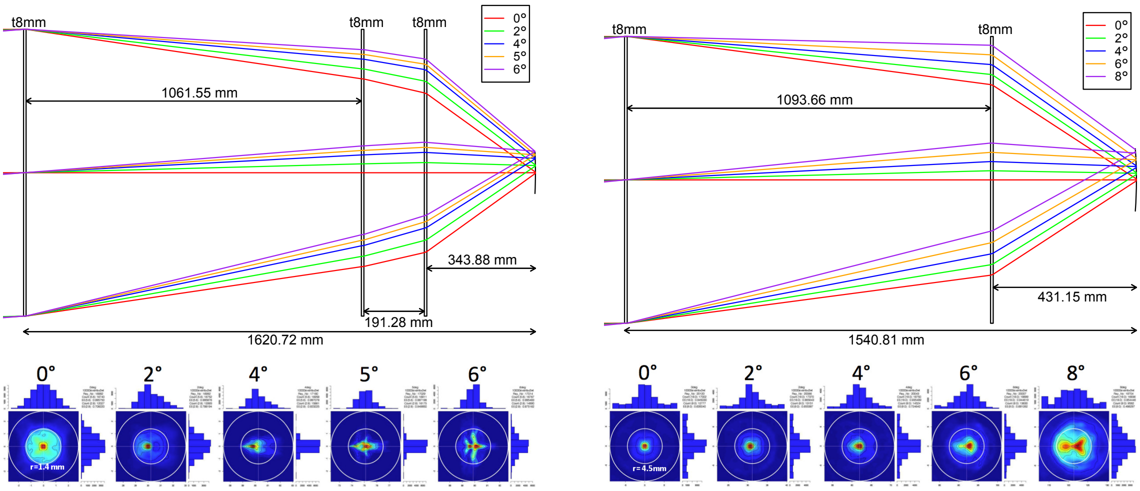

Figure 3.3: Comparison of the optics design from EUSO-Balloon (left) and EUSO-TA (right). The front- and rear-lens design is shared between the two projects, and a middle-lens was added to the EUSO-Balloon optics to fulfill the requirement of the smaller RMS spot size. The size of the inner circles in the spot diagrams are 1.4 mm for EUSO-Balloon and 4.5 mm for EUSO-TA. (Images: Takizawa et al., 2013)

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[6] The FoV of one pixel of the TA fluorescence detector is 1°. This corresponds to 9.6 × 9.6 pixels of the PDM of EUSO-Balloon and is approximately the size of an MAPMT including the dead space.

[7] These focal lengths are only reference values, due to the non-stigmatic images produced by a single lens.

also Section 3.3.1), the rear-lens is sealed to form together with the instrument booth a water-tight compartment for the electronics. Therefore, the rear-lens is fixed in position, while the front- and middle-lens can be adjusted along the optical axis in order to perfectly adjust the lens-positions. More details are given in Santangelo et al., 2012 and Takizawa et al., 2013.

Unfortunately, due to a manufacturing problem, the middle-lens could not achieve the required performance and ray-tracing simulations even showed that the performance of the whole optical system will be better without the middle-lens. Therefore, the middle-lens was removed during the integration campaign in Toulouse and the original 3-lens design had to be reduced to a 2-lens configuration for the first flight, as it can be seen in Figure 3.2. For this 2-lens flight configuration, the RMS spot size was measured to be ~9 mm, which corresponds to 3 × 3 pixels (Catalano et al., 2015).

3.3.3 Electronic Subsystem

The water-tight instrument booth contains the entire electronics of the EUSO-Balloon instrument. A functional block diagram of the instrument is given in Figure 3.4. The main components are the Photo-Detector Module (PDM) and the Data Processor (DP), which are completed by a PoWer Pack (PWP), the telemetry system *Système d'Interface REseau NOSYCA* (SIREN)[8], and instrumentation from CNES like the environment monitor *Instrumentation Chaîne De Vol* (ICDV) and an Ethernet hub (not shown in Figure 3.4). Thus, to fulfill the A-level requirement (see Section 3.2.1) the instrument implements all the key-technologies from JEM-EUSO, but on a smaller scale.

The two components of the electronic subsystem with the most relevance for this thesis – namely the PDM and the DP – are described in more detail in the following sections.

3.3.3.1 Photo-Detector Module

As already introduced in Section 2.3.2, one PDM, which is the basic detector unit from the JEM-EUSO FS, is used as a detector for EUSO-Balloon (see also Section 2.3.2). It is hierarchically assembled from 9 ECs, which in turn are composed of 4 MAPMTs. Each MAPMT has 64 dedicated anodes in an 8 × 8 array, which results in 48 × 48 pixels for the EUSO-Balloon detector. The main specifications of the MAPMT are given in Table 3.1 (see also Section 2.3.2 for further information).

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[8] NOuveau SYstème de Contrôle d'Aérostats (NOSYCA)

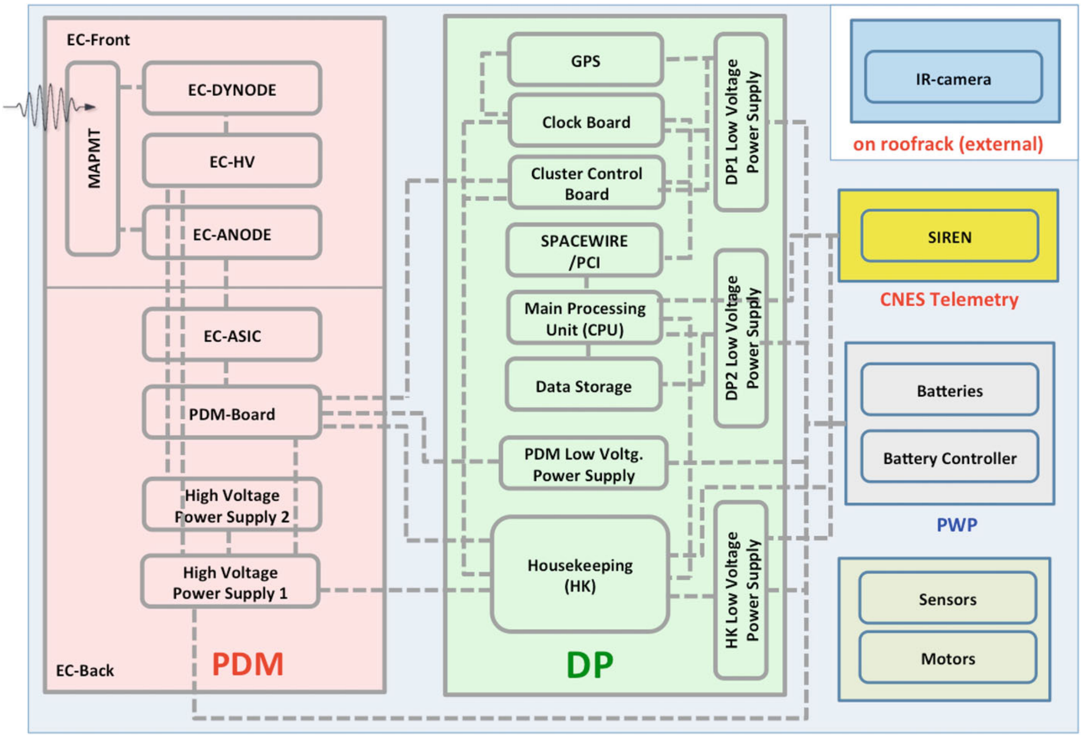

Figure 3.4: Block diagram of the EUSO-Balloon instrument, showing the various subsystems and their interfaces. The two main systems are the PDM and the DP and the instrument is completed by the PWP and the telemetry electronics. The IR camera is an independent subsystem and shares only a mechanical interface with the instrument. (Image: Adams et al., 2015d)

The analog to digital conversion of the signals coming from the MAPMTs is performed by an ASIC which was developed for JEM-EUSO by Omega[9]. As this is the same ASIC as used for JEM-EUSO, just a brief description is given in the following paragraph, while its functionality is described in more detail in Section 2.3.3.1 and a schematic drawing of the SPACIROC can be found in Figure 2.5.

For each signal coming from one of the 64 anodes, a pre-amplifier with adjustable gain amplifies the signal, and the following discriminator stage rejects pulses below a configurable threshold. For evaluation purposes and detailed adjustments, this version of the SPACIROC contains three different discriminators, which are supplied either directly from the pre-amplifier, by a fast, or by a very fast signal shaper. These discriminated pulses are then used as trigger signals for digital counters, which are adding up the pulses during a specified time window – the GTU, which is set to

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[9] Omega is a CNRS-IN2P3-Ecole Polytechnique microelectronics design center near Paris.

Table 3.1: Main specifications of the R11265-M64 MAPMT (JEM-EUSO Collaboration, 2010).

Pixel size	2.88 mm × 2.88 mm
Pixel pitch	2.88 mm
Sensitive area	23.04 mm × 23.04 mm
Physical dimensions	26.2 mm × 26.2 mm × 20.25 mm
Mass	27.3 g
Wavelength	330 nm to 400 nm
Quantum efficiency	> 35 % (maximum 40 %)
Gain	order of 10^6 @ 0.9 kV
Anode pulse rise-time	∼1.5 ns
Cross-talk between pixels	∼1 %
Operating temperature	−10 °C to +30 °C
Magnetic field effects	0.1 relative gain variation @ 2 G
Gain degradation after 3(+2) years of operation	81 % (78 %)
Reliability for 3(+2) years of operation	99.1 % (98.5 %)

2.5 µs. These discriminators can easily reject electronic noise, and are therefore the 1st sub-level of the Level 1 (L1) trigger scheme implemented in the PDM electronics (see also Section 2.4). To support a wide dynamic range of the detected light, the SPACIROC also contains a charge integration module (KI) in form of a charge-to-time converter. For this purpose, the KI has 9 inputs: 8 of them are connected to the summed up signals of 8 neighboring channels, and one is routed to the last dynode of the MAPMT and can be used to automatically reduce or switch off the HV to protect the MAPMTs in case of strong light.

The 36 ASICs are placed on 6 'EC-ASIC' boards, which are routing the various analog signals coming via connectors from the MAPMTs to the ASICs and the digital signals from the ASICs to the connectors. The latter are used to connect the 'EC-ASIC' boards to the PDM control board.

The tasks of the PDM control board are to read out the digital data from the ASICs and to evaluate the L1 trigger. This functionality is implemented inside an FPGA, together with various other interfaces, like the scientific data interface to the DP via the CCB (see Section 3.3.3.2). Other interfaces are the configuration interface of the ASICs, the engineering data interface to the HK module, and the interface to the

High-Voltage Power Supply (HVPS).

The high voltages needed by the photocathode, the 12 dynodes, and the grid of the MAPMTs are generated by a high-voltage multiplier (also known as Cockcroft-Walton generator), because a classical voltage divider would consume too much power for JEM-EUSO (see also Bacholle et al., 2015). The HVPS was set to 950 V (between photocathode and anode), which results in a gain of the MAPMT of 1.1×10^6. The voltage of the photocathode can be changed in three steps, which decreases the efficiency of the MAPMT by a factor of around 100 each step. This switching is controlled by the PDM control board in case of too much light in order to increase the dynamic range.

The whole PDM was mounted on a translation stage which allowed to fine-tune the focus during integration, which was essential to be able to switch over from the 3-lens design to a 2-lens design. The complete front-end electronics and the PDM control board are designed to be contained in a volume of 17 cm × 17 cm × 20 cm and, therefore, fit behind the area of the 6×6 MAPMTs, which is 16.5 cm × 16.5 cm. This allows for the modular design of JEM-EUSO and its focal surface layout without increasing the dead-space between the single PDMs.

3.3.3.2 Data Processor

The DP sub-assembly (see Figure 3.5) consists of various modules: e.g., the CPU, data storage, CCB, GPS module, Clock Board (CLKB), and HK. The DP is connected to the PDM via the CCB, which receives the scientific data in case of a positive L1 trigger or on request by the CPU. After processing the L2 trigger algorithm (see Section 2.4) to further reduce the data, the CCB sends the data to the CPU. At the same time, the CLKB collects and provides various information with the help of the GPS module. This information includes not only the current position and time, but also the live- and dead-time of the instrument. In addition, the CLKB also implements several operational modes based on the Pulse Per Second (PPS) signal from the GPS module, which allows to synchronize the data acquisition with the different light sources installed on the helicopter (see Section 3.2.3). The interface for the CCB and the CLKB to the CPU is based on the SpaceWire standard from ESA, and a commercially available SpaceWire to Peripheral Component Interconnect (PCI) adapter card is used, which was modified to comply with the extended temperature range requirement. Finally, the CPU collects the scientific data, manages the data storage, and handles the telecommand and telemetry interface with the SIREN module from CNES, which provides the downlink to the Ground Support Equipment (GSE).

An additional module of the DP sub-assembly is the HK, which collects engineering data from the instrument and its various modules. These data are used to monitor the overall health status of the instrument and include not only voltages, currents, and temperatures, but also comprise various status information of the different

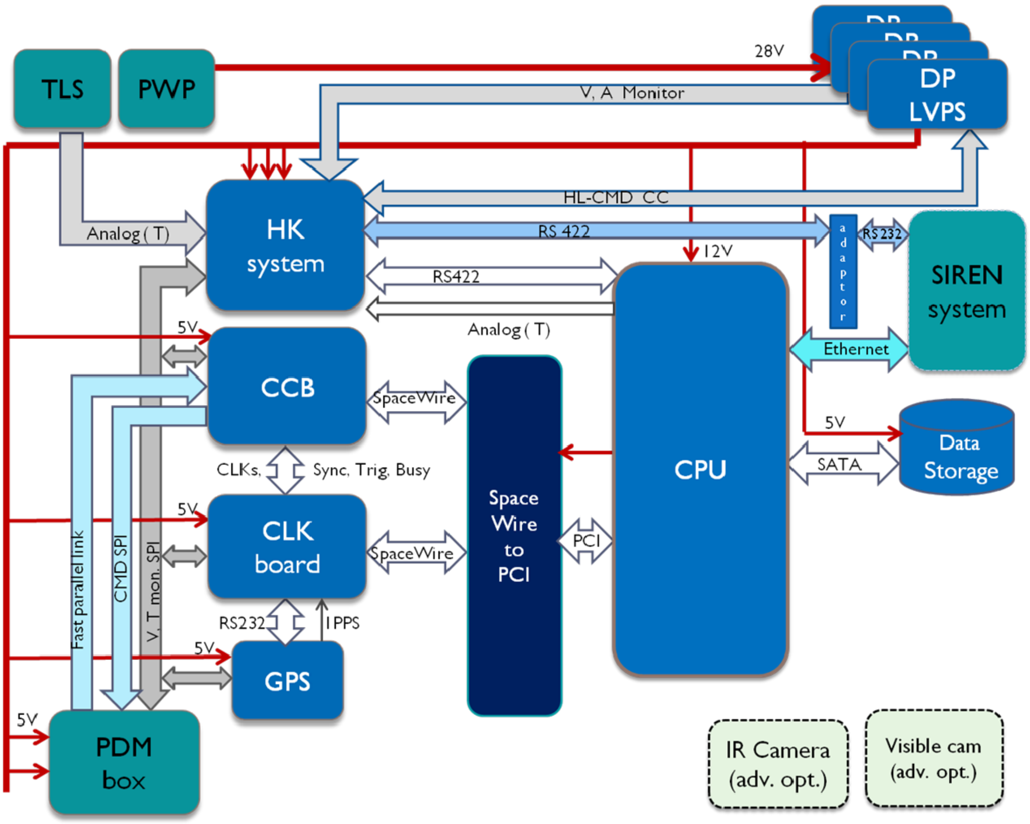

Figure 3.5: Block diagram of the DP sub-assembly showing the various subsystems and their interfaces. (Image: Osteria et al., 2015)

modules, in case of problems with interfaces for example.

Also mounted in the same mechanical support structure and therefore part of the DP sub-assembly are the Low Voltage Power Supplies (LVPSs), which are generating and conditioning the various secondary voltages from the primary voltage delivered by the PWP. More information on the DP and its performance can be found in Osteria et al., 2015.

3.4 The EUSO-Balloon Flight

The launch campaign in Timmins (Ontario, Canada) started on August 12th, 2014, with the final (re-)integration of the instrument after its shipment from Europe. After one week, the flight configuration was reached in the evening of August 18th, 2014. This was important, as the first launch window for EUSO-Balloon opened on the 21st of August, and closed on the 29th. This window was selected around the

Figure 3.6: EUSO-Balloon flight train just before the launch (top). The instrument (on the left) is hanging on auxiliary balloons which support the main balloon (on the right) during the first phase of the launch. The launch of the EUSO-Balloon instrument (bottom left) took place on August 25th, 2014, at 0:53 UTC from Timmins (Ontario, Canada). After 4.62 h at float altitude, the instrument was recovered from a small lake around 100 km west of Timmins (bottom right). (Images at the bottom: Adams et al., 2015d)

new moon on August 25th.

After a positive system check-up inside the hangar on the evening of August 24th, the instrument was ‘rolled-out’ to the tarmac of Timmins Airport around 22:00 UTC and the flight preparations started. While already hanging on the auxiliary balloons, the final health test of the instrument was performed, which also included the complete telemetry and all parts of the flight train. Auxiliary balloons held the payload until the main balloon would have been released, and supported the main balloon during the first launch phase. Since the protective cover of the front-lens was sealed and light tight, a full end-to-end test of the instrument could be performed, including the switching on of the HVPS and monitoring the status of the MAPMTs. After this successful final test, the main balloon was unfolded and filled with helium.

The release of the balloon – the most critical phase during a balloon flight – took place at 0:53 UTC, and the 467 kg heavy EUSO-Balloon was smoothly lifted up (see Figure 3.6). Shortly after the launch, the auxiliary balloons were separated from the

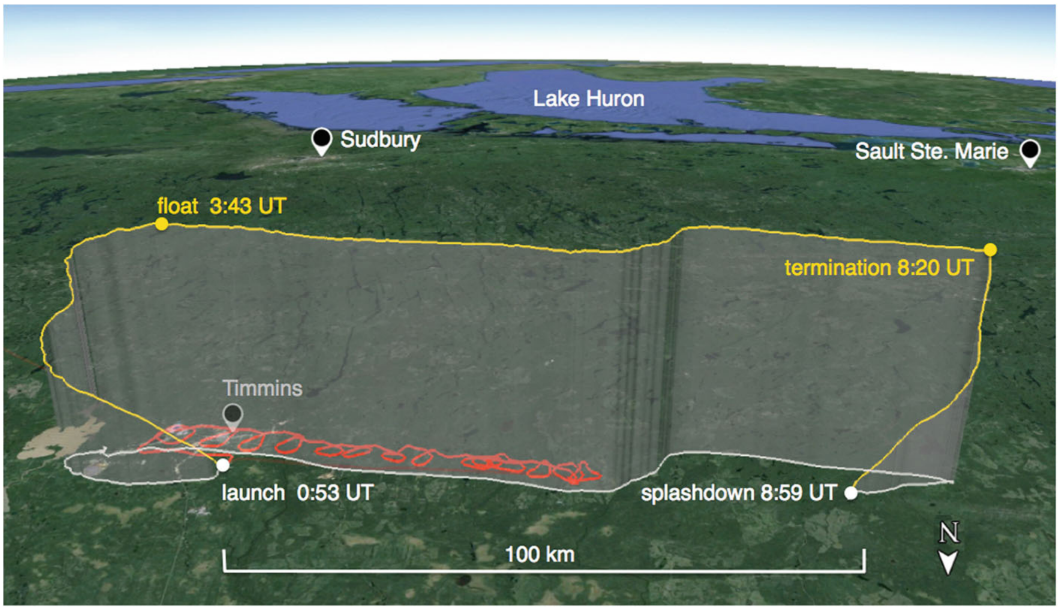

Figure 3.7: Flight path of EUSO-Balloon (yellow) and its on-ground projection (white). Also shown is the track of the helicopter (red) which followed the instrument for 2.28 h. (Image: Adams et al., 2015d)

gondola as they are only needed during the very first phase of the launch. The ascent ended nearly 3 h later, when the float altitude of 38.3 km was reached at 3:43 UTC. Already during the last part of the ascent, at an altitude of 32 km, the data from the photodiodes showed that it was dark enough at the instrument's location to safely switch on the detector, and the high voltage for the MAPMTs was ramped up at 2:50 UTC. The data which were arriving in the control room at the Timmins Airport showed that all systems were alive and working properly.

Just before reaching float altitude, the helicopter came into the FoV of the instrument and followed the balloon for 2.28 h at an altitude of 3000 m. During that period, the light sources were fired around 150 000 times to generate different events (see also Section 3.2.3 and Eser et al., 2015). The flight paths of the instrument (in yellow) and of the helicopter (in red) are shown in Figure 3.7.

After 4.62 h at float altitude, the end of the astronomical night was reached and, in order to deploy the parachute, the instrument was separated from the balloon to start its descent into one of the 'driest' landing zones available since launch. Hanging on the parachute, the descent ended after nearly 40 min at 8:59 UTC in the middle of a small lake, around 100 km west of Timmins (see Figure 3.6).

The recovery of the instrument and the flight train was done with the help of a helicopter, which lifted the instrument out of the lake and placed it on a trailer for the transportation back to the hangar at the launch base. Thanks to the built-in security measures (see Section 3.3.1), the instrument booth and the IR camera were undamaged, and the electronics dry and working. The complete flight data were successfully recovered from the disks, and a total of 258 592 data packets were recorded with the main instrument. This corresponds to roughly 33 million UV pictures with all kinds of ground covers like soil, vegetation, open water, urban areas, and different kinds of clouds (Adams et al., 2015d). A total of 270 artificial 'CR events' – generated by the laser on-board the helicopter – were recorded, mainly during periods when no clouds where present under the instrument (Eser et al., 2015). The IR camera took overall 753 pictures during a total operating time of around 17 h, of which around 220 were taken while the instrument was at float altitude (Rodriguez Frias et al., 2015).

With this amount of gathered data, the good performance of the electronics and instruments, and the safe recovery of the payload after the splash-down, the EUSO-Balloon project can be considered as completely successful.

4 EUSO-SPB

Soon after the successful launch of EUSO-Balloon, ideas for successor flights had been developed. One option was to carry out a similar flight as EUSO-Balloon with sea-recovery, again in collaboration with CNES, who re-opened their launch site in Aire-sur-L'Adour, France. The other possibility was to perform an ultra-long duration flight on board a Super-Pressure Balloon (SPB) in collaboration with NASA, with a launch from their recently opened launch site in Wanaka, New Zealand.

As an ultra-long duration flight can last several weeks[1] at float altitude, the second option provided the possibility to detect cosmic ray induced events and was therefore prioritized by the collaboration. After a short preparation and development phase of around two years, EUSO-SPB was launched in April, 2017 (see Figure 4.1). Unfortunately, the balloon developed a leak which led to an early termination of the flight: already twelve days after its launch, the instrument was slowly descended and impacted in a controlled way into the South Pacific Ocean, around 375 km south-east of the Easter Island, – this procedure is called ‘valve down’.

This chapter gives an introduction to the EUSO-SPB mission, explains the concept of SPBs in general, and emphasizes the differences and improvements of the EUSO-SPB instrument with respect to EUSO-Balloon.

4.1 Objectives and Requirements

While the pathfinder mission EUSO-Balloon had its main focus on the proof of concept, technical feasibility, and background determination, EUSO-SPB's main objective was the gathering of scientific data. L. Wiencke et al. (2017) states the mission objectives as follows:

- In fact, EUSO-SPB fulfills all criteria to become the first mission ever to observe UHECR induced EASs by looking downwards with a fluorescence telescope.

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[1] The current record for a mid-latitude flight was set in 2016 with a project called Compton Spectrometer and Imager (COSI) as scientific payload, which was 46 days aloft. The overall record was set in 2013 with the experiment Super Trans-Iron Galactic Element Recorder (SuperTIGER) and a flight duration of 55 days, launched from Antarctica.

Figure 4.1: The EUSO-SPB instrument hanging on the launch vehicle (foreground, left) just before its launch on April 25th, 2017, at 23:51 UTC from Wanaka Airport, New Zealand. The Super-Pressure Balloon (background, right) with a volume of $532\,000\,\mathrm{m}^3$ will reach a float altitude of 33 km and is currently being filled with helium. (Image: NASA/Bill Rodman)

- It will measure the background UV light at night for different environmental preconditions, e.g., when passing over oceans or the influence of clouds. An accurate background estimation is the basic requirement for any interpretation of scientific data and thus plays a major role in this mission.
- It will search for fast UV pulse-like signatures from objects others than UHECRs. Such signatures can originate from Meteoroids or TLEs and will provide more information of their properties like occurrence, size, and origin.

Apart from these scientific aims, another main objective of the mission is to further improve and raise the TRL of the subsystems like the Front-End Electronics (FEE), the read-out electronics, and the trigger algorithms, which are the pathfinders for downwards-looking UHECR telescopes.

After considering the mission characteristics like estimated flight duration, field of view, detector sensitivity, and background estimation, the success criteria of the EUSO-SPB mission were defined as follows by Wiencke et al. (2016):

- observation of >10 air showers induced by UHECR (i.e., $E_{particle} > 10^{18}\,\mathrm{eV}$);

- detection of at least one air shower with Cherenkov back-scattered light.

Based on the expected number of events (Bacholle et al., 2016; Fenn, 2015), these detections require a minimum of 20 nights around new moon, 100 h of observation time, and a float altitude of 30.5 km. An under-flight with an aircraft, equipped with various light sources similar to the helicopter under-flight of EUSO-Balloon (see Section 3.2.3), was regarded as highly desirable. These level 1 minimum requirements for the mission are accompanied with comprehensive requirements, for which the following guidelines were set (Wiencke et al., 2016):

- duration of flight: 100 days,
- observation time: 500 h,
- float altitude: 36.6 km,
- under-flight: 4h,
- successful recovering of the instrument.

Because of the planned ultra-long duration flight and the high sensitivity of the instrument, also the discovery potential of previously unmeasured phenomena cannot be neglected.

4.2 Technical Aspects of EUSO-SPB

As EUSO-SPB was the successor of EUSO-Balloon, which successfully flew in 2014 and recorded the first artificial 'CR events' (see Chapter 3), there are many similarities between these two instruments, and a few subsystems have been even reused. Nevertheless, based upon the experience obtained during the EUSO-Balloon flight, several improvements have been added. Therefore, the instrument itself is an updated and advanced version of the EUSO-Balloon instrument. The most important technical differences and upgrades implemented in EUSO-SPB are highlighted in the following sections, and a short introduction to SPBs is given.

4.2.1 Super- and Zero-Pressure Balloons

The most fundamental improvement of EUSO-SPB with respect to EUSO-Balloon was the change of the used balloon-system: while EUSO-Balloon was flying with a zero-pressure balloon, EUSO-SPB was launched using a super-pressure balloon. This system allows for a flight duration of up to 100 days, thus greatly enhancing the observational time compared to the one night of EUSO-Balloon.

Zero-pressure balloons (like EUSO-Balloon) have either a vent at the bottom or are simply open. During ascent, the helium expands and, as soon as the complete volume of the balloon envelope is filled, excess helium can escape and float altitude is reached (i.e., $P_{in} = P_{ext}$). Due to the lower temperature during night ('diurnal cooling'), the volume of the balloon will shrink, resulting in a loss of altitude. To maintain the altitude during night, and to avoid a runaway effect because the temperature of the stratosphere is decreasing with decreasing altitude, ballast has to be removed. On the next day, when the helium becomes heated up again, the balloon will ascent higher than on the previous day, as the system is now lighter, and thus more helium will escape. The released ballast is typically of the order of 6 % to 8 % of the system's mass per day, which sets an obvious limit on the flight duration – when all ballast is used up, the balloon will eventually come down.

In contrast to zero-pressure balloons, super-pressure balloons are closed and thus prevent a helium release (i.e., $P_{in} > P_{ext}$). If the internal pressure is high enough, the diurnal heating and cooling changes only the pressure but not the volume of the balloon.[2] Therefore, a super-pressure balloon continues to float at the same density altitude and thus does not suffer from a loss of altitude during night. As no diurnal ballast is necessary and no helium is released, the flight duration of super-pressure balloons can take up to several weeks.

While being at float altitude, the EUSO-SPB is kept on its high-latitude track by strong circumpolar winds, which will guide the balloon around the globe once every few weeks. These winds, blowing from west to east, develop once per year over the southern ocean and can be reached by a balloon from the launch site located in Wanaka, New Zealand.

For EUSO-SPB, the pumpkin-shaped balloon has a maximum payload mass of $\sim 2.5\,\mathrm{t}$, a volume of $532\,000\,\mathrm{m}^3$, and a float altitude of 33 km.

4.2.2 EUSO-SPB Gondola

For the balloon gondola, the well-established EUSO-Balloon mechanical structure was enhanced with an additional exoskeleton to support the solar panels and the various instrumentation from CSBF[3] like the ballast hoppers or the Support Instrumentation Package (SIP) together with antennas for communication and navigation (see

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[2] The pressure inside the balloon is chosen to be high enough, so that even during the diurnal cooling over night the pressure inside is still higher than the surrounding atmospheric pressure. Therefore, the volume of the balloon envelope is still completely filled.

[3] The Columbia Scientific Balloon Facility (CSBF) is a NASA facility based in Palestine, Texas, which is responsible for various services around high-altitude research balloons. These services are not only related to the launch and recovery of balloons, but also include all necessary preconditions like flight preparations, site selection, and logistics.

Figure 4.2: The EUSO-SPB gondola during the final integration in Wanaka, New Zealand, (left) and in flight-ready configuration (right). The flight-proven gondola of EUSO-Balloon (red) is mounted inside an exoskeleton, which provides mechanical support for the various instrumentation from CSBF (located above the EUSO-Balloon gondola) and for the solar panels.

Figure 4.2). The exoskeleton is constructed in a way that the EUSO-Balloon gondola (with removed floaters and crash pads) can be slid into it and is then fixed to it. This system allows an independent and parallel integration of the scientific instrument and the CSBF instrumentation, thus simplifying and accelerating the final assembly.

Due to the long duration of the flight, solar panels have been added to charge the batteries during daytime. To provide the necessary power for the instrument, three flight-proven (by CSBF) solar panels with a nominal power capacity of 100 W each were attached to the crinoline or ‘skirt’ of the gondola, and additional four panels were mounted to power the instrumentation from CSBF. Their power capacity is based on a deep worst case analysis which also includes various factors like launch date, temperature, or imperfect orientation to the Sun. Since EUSO-SPB does not possess a stabilization system for the rotation of the gondola, all four sides of the instrument are equipped with solar panels.[4] In case of a planned flight-termination over land, the crinoline also acts as a crash pad.

To store the power generated by the solar panels during daytime, a battery pack consisting of 14 batteries is used. Theses batteries are Absorbent Glass Mat (AGM)-type 12 V batteries (Odyssey PC1200), which are also flight-proven by CSBF. The battery pack is organized as 2S7P, i.e., two batteries are connected in series to form a pair with a nominal voltage of 24 V, and seven pairs are connected in parallel. This battery pack has a total capacity of 224 A h at 0 °C and a weight of ~ 250 kg.

In contrast to EUSO-Balloon, the EUSO-SPB gondola is not designed for a sea recovery. On the contrary: due to naval safety requirements, the design of the gondola has to ensure that it will act as a kind of anchor for the balloon envelope and that it will cause the full flight train to sink onto the ground in case of an early termination over the ocean – which was actually the case for EUSO-SPB.

4.2.3 EUSO-SPB Optics

As the mechanical structure of EUSO-Balloon has been reused, the telescope subsystem of EUSO-SPB also uses the same optics design (see Section 3.3.2). However, a new set of lenses was manufactured, and particularly the middle diffractive lens had been improved. Based on the successful recovery of EUSO-Balloon, the 'old' lenses were still available and regarded as a backup solution, e.g., in case of damage during transportation. A comparison of the trigger efficiency between the 2-lens and the 3-lens configuration has been performed during the field tests (see Section 6.5.4.1). This evaluation of the trigger efficiency showed that for the 2-lens configuration – despite its larger RMS spot size of around 10 mm – a factor of 2 less energy from the mobile Ground Laser System (GLS) was necessary to achieve 50 % trigger efficiency (Bayer et al., 2017; L. Wiencke et al., 2017). The reason for this is that the total light throughput is a factor of 2.5 higher for the 2-lens configuration – which is 30 % compared to 12 % for the 3-lens system (J. Eser et al., 2017). Based on these measurements, it was decided to fly with the 2-lens configuration, as was also the case for EUSO-Balloon.

4.2.4 EUSO-SPB Electronics Subsystem

After the EUSO-Balloon flight, a list was compiled which included all the possible improvements which could be implemented in the electronics for a successor flight. Due to the relatively short time schedule, which at the beginning also included an

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[4] In general, the use of a four-sided solar array is standard even if the balloon is equipped with a rotator, to provide some degree of redundancy in case of a failure of the stabilization system.

additional flight similar to the previous one, again in collaboration with CNES in 2016, the most important items were selected based on the available time, manpower, and costs. The following sections highlight several important changes of the electronic subsystem in comparison to the EUSO-Balloon electronics.

4.2.4.1 Photo-Detector Module

Most of the improvements were implemented into the PDM based on two main motivations: first, to improve the performance of the detector in general, and second, to further raise the TRL of the basic detector unit towards a space mission like JEM-EUSO.

One of the biggest achievements, which can be regarded as a milestone towards the space qualification of the PDM, was the redesign of the HVPS. For EUSO-SPB, it is integrated and potted into the EC, thus greatly reducing the overall size and mass, which are critical properties for space experiments. At the same time, this simplifies the routing of the HVs to the dynodes of the MAPMTs. This was important, to avoid the risk of a possible failure associated with the low-pressure environment at float altitude, which had been depicted during the preparation of the EUSO-Balloon flight. Due to the potting, the nominal voltage between the photocathode and the anode could be increased to 1.1 kV, which also increases the gain of the MAPMT. The basic design of the HVPS is the same as for EUSO-Balloon and is based on a 'Cockcroft-Walton' voltage-multiplier or 'Villard' cascade (see Plebaniak et al., 2017, for more details). The enhancement of the EC also includes an advanced MAPMT, which provides a higher quantum efficiency.

An additional improvement was the usage of a new version (i.e., the third generation) of the SPACIROC as FEE. The central advancement of the third generation of this ASIC is a higher double pulse separation of better than 10 ns to avoid pile-up during conditions with more light. At the same time, the power consumption could be reduced to < 0.8 mW/channel. More details on the SPACIROC 3 are given in Blin et al., 2018. Together with this new ASIC, also the 'EC-ASIC' boards have been revised to implement a better grounding, which reduced the noise from the electronics.

Last but not least, several improvements were implemented on the PDM control board (see Section 5.3):

(1) a different FPGA was installed, which provided more resources,

(2) the Power Distribution Network (PDN) was enhanced,

(3) a completely new thermal dissipation system was developed, and

(4) the configuration or firmware of the FPGA was re-written and highly optimized to implement additional functionalities which was not available for the EUSO-Balloon flight.

More details on the improvements and the new implementation of the PDM control board, which were all done within the scope of this thesis, can be found in Section 5.3.

4.2.4.2 Data Processor

Due to the possibility of a long duration flight of several weeks, the DP and especially the flight software were greatly enhanced with the goal of a (nearly) autonomous instrument. In addition, the DP required new command- and data-interfaces with the GSE and has now also to monitor and control several additional auxiliary devices (see Section 4.2.4.3). To handle all these tasks, a more powerful flight computer was selected, which is based on the AMD Fusion G-Series APU high performance processor and incorporates a 1 GHz Dual-Core CPU. For more details on the new DP and its control- and data-software, see Osteria et al. (2017).

The communication with the instrument has to be possible during the entire long duration flight of the balloon. As EUSO-SPB travels around the globe, the direct line-of-sight communication – which was available for EUSO-Balloon and which has a rather high bandwidth – is only available during the first few hours after the launch. Therefore, the main communication channel with the scientific payload is done via two redundant Iridium Pilots, which can be used in parallel and provide a maximum bandwidth of $70\,\mathrm{kbit\,s^{-1}}$ each. In addition, the SIP provides two redundant low-bandwidth downlink channels via the TDRSS[5] and one uplink port via the Iridium network. For more information on the communication with the scientific payload, see Orbital ATK Inc., 2016.

As another lessons-learned from EUSO-Balloon, EUSO-SPB is equipped with a second, redundant GPS receiver, to ensure a solid position and time determination of the balloon and its gathered data. This is especially vital for EUSO-SPB due to its long flight duration and the large distance traveled. An additional differential GPS receiver (‘Compass’) was added, which provides accurate information on the absolute orientation of the instrument during the flight.

4.2.4.3 Auxilary Devices

As it was the case for EUSO-Balloon, a few additional instruments and devices were added besides the main instrument, which are briefly described in the following.

SiECA A first prototype of a Silicon PhotoMultiplier (SiPM) camera was added to the FS of EUSO-SPB – the Silicon photomultiplier Elementary Cell Addon (SiECA). SiPMs are an emerging alternative to traditional photomultipliers for the detection

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[5] The Tracking Data Relay Satellite System (TDRSS) is a network of communication satellites which is used by NASA to communicate with satellites and the ISS.

of single photons. They operate at much lower voltages (of the order of 30 V to 50 V), are not susceptible to damage in case of too much light, and are much lighter and more compact. Because of these advantages, SiPMs are a promising option for a future replacement of the detector.

The detector of the installed SiECA consists of four SiPMs with 64 channels each (Hamamatsu S13361-3050AS-08), arranged in a 2 × 2 array to resemble one EC from the PDM. The read-out and signal conditioning is done by a dedicated ASIC (Weeroc Citiroc 1A). The control electronics is implemented inside an FPGA, which is accompanied by special voltage generators which are providing the bias voltages for the SiPMs. More details on the development and performance of SiECA are given in Painter et al., 2017.

UCIRC As for EUSO-Balloon, the main instrument was accompanied by an IR camera to determine the atmospheric conditions inside the FoV of the main UV camera. It is particularly important to determine the presence of clouds and their top heights, as they can influence the amount of light detected by the main instrument and, therefore, might cause an inaccurate reconstruction of the shower parameters. In addition, the knowledge of the presence of clouds is important to determine the exposure of the instrument, as showers can develop below clouds and can thus be possibly invisible to the detector.

Due to the planned long flight duration, it was not possible to use the autonomous camera from the EUSO-Balloon mission. Therefore, a new camera was developed – the University of Chicago Infrared Camera (UCIRC) – which interfaces with the DP, allowing the transfer of data to ground and to command and monitor the camera. The EUSO-Balloon IR camera used one camera with two filters which split the sensor into two regions, sensitive to two different wavelengths bands. In contrast to this design, the UCIRC consists out of two cameras, each having its own bandpass filter and optics – one for the 10 µm- and one for the 12 µm-band. The FoV of the UCIRC (32° × 24°) is larger than that of the main UV camera (11.1° × 11.1°). Therefore, atmospheric data inside the FoV of the main camera are also available between two successive exposures of the IR camera. This is important since the IR camera only takes one picture every minute.

To keep the two cameras at a stable temperature during the data-taking phase, a dedicated temperature control- and monitor-system was implemented, which uses Peltier elements, resistive heaters, and heat-pipes to keep the temperature stable. A detailed description of the UCIRC can be found in Allen et al., 2017.

Health-LED At the center of the rear-lens (L3), a UV LED was installed which can illuminate the whole PDM (and the SiECA). This ‘Health LED’ is controlled via command and, once activated, is firing twice every 16 s with a calibrated pulse-length and -height. These pulses were used during the flight by the operators to quickly evaluate the overall 'health' status of the instrument and to monitor the long term stability of the PDM. In addition, the LED can be put into a 'DC' mode, to illuminate the PDM with a constant amount of light. In this mode, the 'S-curves' were measured, which deliver information on the gain of the MAPMT. The long-term evolution of this gain is important to evaluate the degradation of the photocathode and to adjust the trigger thresholds of the SPACIROC.

Radiometers As the radiometer installed on EUSO-Balloon proved to be useful, a similar system was mounted to the EUSO-SPB instrument. Two redundant photodiodes[6] – calibrated by the National Institute of Standards and Technology (NIST) – were installed at the side of the PDM and could be read-out by telecommand. During the long duration flight, it was especially important to estimate the amount of light reaching the instrument. This information was used by the operators during the day-night and night-day transitions to safely start and stop data acquisition without damaging the MAPMTs.

Tracker beacon An under-flight with an airplane, equipped with different light sources, was planned for EUSO-SPB – similar to the helicopter under-flight of the EUSO-Balloon campaign. Therefore, a similar system of a tracker beacon was installed, to locate and follow the balloon's trajectory during one of the first nights after launch or when the balloon would have concluded one orbit. Unfortunately, the under-flight was canceled due to the early termination of the flight. More details on the in-flight calibration system and the under-flight is given in M. Mastafa et al., 2017.

4.3 EUSO-SPB Field Tests

In preparation of the 'hang test' (see Section 4.4) in Palestine (Texas, USA), the instrument was extensively tested at the TA site 'Black Rock Mesa' near Delta (Utah, USA). The fully assembled instrument was transported from Golden (Colorado, USA) – where the instrument had previously been integrated – to this field test campaign, in a customized trailer with air suspension. This trailer was chosen to keep the lateral vibrations of the instrument at a minimum.[7]

At the same time, the trailer acted as an enclosure on-site and as 'dark box' during the day. During the night, the rear doors of the trailer were opened and

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[6] Based on the positive experience during the EUSO-Balloon flight, the same sensor (PD300-UV) was used together with a 'Nova II' radiometer from Ophir.

[7] While the instrument was built to withstand a shock of up to 10 g during the opening of the parachute along the optical axis, it is not built to withstand strong lateral shocks.

the instrument was operated while staying inside the trailer and was tilted by 7.8° towards the night sky. As the EUSO-SPB instrument was positioned beneath the EUSO-TA prototype, parallel observations with both instruments could be performed.

The calibration of the instrument and the evaluation of its performance was realized with several light sources at different distances from the EUSO-SPB instrument:

1. The trigger efficiency was evaluated with the help of the prototype of the GLS. This steerable laser system was mounted on another trailer at a distance of 24 km and is able to produce artificial 'air showers' with defined energy and direction inside the complete FoV of the instrument.

2. An absolute calibration was performed with a calibrated and temperature stabilized 365 nm UV LED, mounted on a mast at a distance of 45 m.

3. A cross-calibration with the TA project can be realized using the data recorded from the Central Laser Facility (CLF), which is located at a distance of 21 km and is used for the calibration of the TA fluorescence telescopes.

4. The data from the CLF in conjunction with those from the GLS were also used to estimate the amount of aerosols in the air, which can influence the trigger efficiency measurements and especially affects the comparison between the 2-lens and the 3-lens configuration, for which the measurements had to be done during two different nights.

5. Stars were used together with the laser system to measure the final FoV of the instrument.

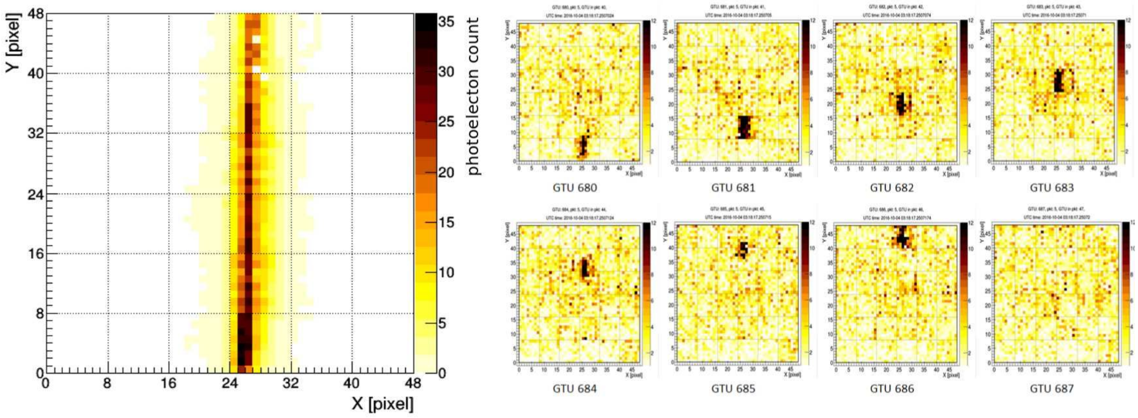

Figure 4.3: The left picture shows the average of 271 integrated laser pulses from the TA CLF which were recorded during the EUSO-SPB field tests. On the right side, a GTU by GTU sequence of a single laser pulse is shown, as it travels through the field of view of the instrument. (Image: Eser, 2018)

During the one week of field tests, the instrument was thoroughly tested, and especially the performance of the new implementation of the L1 trigger algorithm (see Section 2.4.1) was successfully evaluated with hundreds of thousands of laser shots. The energy threshold at 50 % trigger efficiency was determined to be 3×10^{18} eV for an EAS inclined by 53° and observed from a distance of 33 km (Bayer et al., 2017). More details on the trigger performance can be found in Section 6.5.4.1

The preliminary absolute photometric calibration, obtained from thousands of light flashes from the UV LED during the field tests, was measured to be 0.078 ± 0.010 photoelectrons per incident photon – which is in agreement with the laboratory measurements performed during the integration.

Applying the two methods mentioned above under (5.), the FoV measured with stars is $(11.10 \pm 0.15)°$, and from the measurement with the laser sweep, it was found to be $(11.2 \pm 0.1)°$ (J. Eser et al., 2017). More details on the transportation of the instrument and on the field tests are given in Cummings, 2017, Eser, 2018 and J. Eser et al., 2017.

4.4 The EUSO-SPB flight

After the field tests, the instrument was transported to CSBF in Palestine (Texas, USA) for the 'hang test', which was passed successfully on November 19th, 2016. During the 'hang test', the functionality of the assembled instrument in flight configuration has to be demonstrated. This is an end-to-end test including the telecommand system while the instrument is hanging on a crane, to simulate its hanging on the balloon during the flight. Additionally, this is also an electro-magnetic compatibility test, to see if the radio transmission is interfering with the electronics or the detector of the instrument. After the successful 'hang test', the instrument was again disassembled and packed into two sea containers for its shipping to New Zealand.

Around two months later (end of January, 2017) and after the Mission Readiness Review on January 18th, the instrument and equipment arrived at the airport of Wanaka (Otago, New Zealand), and the final assembly and flight preparations started. After several weeks of work and efforts from the on-site team – which included the complete disassembly of the main UV camera due to a transportation damage, a final cleaning of the lenses accompanied by a flat-fielding of the detector, mechanical work, and the thermal isolation of the instrument – a last 'hang-' and compatibility-test was performed. Finally, the flight readiness review was successfully passed on March 24th, 2017.

From that day on, the weather and risk was evaluated basically every day, to check if the conditions are good enough for a launch. Several specific conditions have to be fulfilled before a launch attempt (or 'show') is called out. For example, the launch phase is very sensitive to ground winds, as the size of the balloon provides a huge

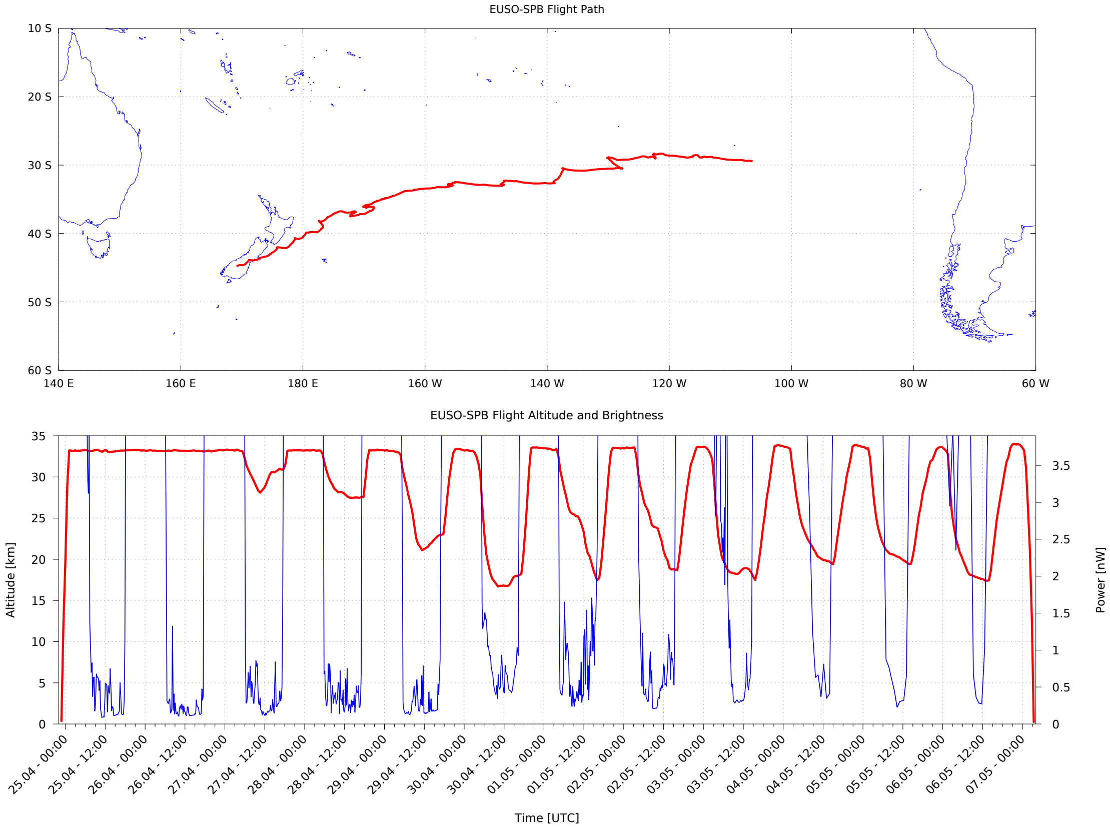

Figure 4.4: Flight trajectory (top) of EUSO-SPB, with its launch on April 24th at 22:49 UTC from Wanaka (Otago, New Zealand) and its splash-down after 12 days of operation on May 7th, 2017 at 03:23 UTC, around 375 km south-east of the Easter Island. As it can be seen from the float altitude (bottom, red) and the brightness recorded by the photodiodes (bottom, blue), the balloon went out of its super-pressure mode during the third night, and from that on suffered from altitude loss during the cold nights. Around 3000 km away from the coast of Chile – which would have allowed a landing and recovery of the instrument – the ballast was used up, and the 'valve down' procedure was initiated.

contact surface for the wind. On the other hand, the trajectory of the balloon after launch should not go over densely populated areas, due to the risk involved in case of a failure – this is especially true during the pressurization phase of the balloon, at which point the pressure inside the balloon starts to exceed the atmospheric pressure for the first time. Thus, stronger winds in the correct direction are necessary at higher altitudes, so that the balloon quickly traverses the land to reach the open ocean.

Eventually, on April 24th, with good weather conditions and the risk analysis just below the set criteria, EUSO-SPB successfully started its journey at 22:49 UTC at its 8th launch attempt.[8] The winds brought the balloon on a trajectory along the east coast of New Zealand, reaching the open sea just around 30 km south of Christchurch.

As the launch was performed one day before new moon, data taking could directly start during the first night, and the 24/7 ground operations were done from shift centers spread around the globe. One center was located at RIKEN in Tokyo (Japan), one at the Colorado School of Mines in Golden (Colorado, USA), and four in Europe: at the University of Tübingen (Germany), at the IRAP[9] in Toulouse (France), at the University of Torino (Italy), and at the University of Naples (Italy). During the first week of the flight, the ground operation shift during the night-time of the balloon – i.e., during the data-taking phase – was done in Tübingen. All instruments were operating within their specified parameters and the data-taking was working correctly.

Unfortunately, during the third night of the flight, the balloon went out of super-pressure mode and showed a loss in altitude – later on, a leak was confirmed. From that time on, EUSO-SPB was basically no longer a super-pressure balloon and more comparable to a zero-pressure balloon – surviving only as long as ballast is available (see Figure 4.4, bottom). As it was clear that the chances of reaching a safe landing spot at the west coast of Chile were low, the priority of the operators was to take and download as much data as possible. Due to the rather low bandwidth (which was reduced even more as one of the two links failed), it was decided to use a higher compression of the data packages by basically removing a part of the recorded data frames, and new software was written and uploaded.

Due to bad weather with extremely cold temperatures – which means that a lot of ballast has to be dropped – the flight termination sequence or 'valve down' was started on the 13th day of the balloon flight. For that purpose, the valve at the top of the balloon is opened from time to time to release the remaining helium. This leads to a controlled descent of the balloon, and is done to bring down the whole flight train, without separating the payload from the balloon or opening the parachute. This is important as the payload has to pull the complete balloon envelope to the ground of the ocean and act as an anchor (as required by naval security requirements). In the end, the splash-down of the instrument occurred on May 7th, 2017, at 03:23 UTC, around 375 km south-east of the Easter Island, and the whole balloon should rest now around 3000 m below sea level. The flight path of EUSO-SPB is plotted in Figure 4.4.

During its 12 days and 4 h of operation, the instrument acquired data for a total of around 40 h during night. This translates to around 60 GB of data which were

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[8] The previous launch attempts had to be canceled due to changes in the weather condition and the resulting increase of the risk level.

[9] Institut de Recherche en Astrophysique et Planétologie

recorded to the disks. Of these data, it was possible to download around 40 GB before the instrument stopped responding. Nevertheless, all instruments of the payload and the (main) detector were operating correctly, and the data acquisition was performed without major problems. Thus, with a longer flight duration, the chances of obtaining the main mission objectives would have been promising.

5 Development of the Camera Electronics

One of the major challenges of the JEM-EUSO instrument is the rather low bandwidth of 300 kbit s^{-1} (JEM-EUSO Collaboration, 2010) allocated to the experiment through the ISS downlink to the GSE. To reduce the huge amount of data produced at the level of the FEE – which is more than 1 Tbit s^{-1} – to a data rate complying with the allocated bandwidth, a trigger scheme with several hierarchical levels was developed (see Section 2.4). This reduction of the data rate can be achieved by discriminating real events associated to EASs from spurious events, as the expected EAS rate is only of the order of 10^{-3} Hz (see Table 2.2), which translates to a data rate[1] of roughly 20 kbit s^{-1}. Thus, the key functionality of the read-out electronics is to keep the spurious trigger rate below a certain level which complies with the data budget.

Within the hierarchical and modular concept of the JEM-EUSO detector (see Figures 5.1 and 2.3), the Cluster Control Boards (CCBs) – together with the PDM control boards – are playing a central role in the data flow and the triggering scheme. In case of an L1 trigger (see Section 2.4.1) from the PDM control board, the CCB reads out the data coming from a cluster of eight or nine connected PDMs and evaluates the L2 trigger algorithm, which is described in detail in Section 2.4.2. In case of a positive outcome of the trigger evaluation, the CCB notifies the MDP and buffers the data until they can be transferred to the on-board storage.

In Section 5.1, the development of a first CCB prototype board is described which was started in Bayer (2011) as a breadboard model on the basis of a Commercial Off-The-Shelf (COTS) board. This breadboard model was important in order to prove the feasibility of the implementation with the chosen architecture – at this stage, special attention was given to the implementation of the L2 trigger algorithm and a fast data interface to transfer the data from the PDM to the CCB. The development of a scaled down version of the CCB for the pathfinder missions EUSO-Balloon and EUSO-SPB is described in Section 5.2, and the re-design of the PDM for EUSO-SPB is presented in Section 5.3.

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[1] Assuming a packet of 128 GTUs of photon counting data from the triggering PDM cluster without any engineering data or data from the AMS: 9 PDMs × 9 ECs × 4 MAPMTs × 64 Channels × 8 bit × 128 GTUs × 10^{-3} Hz ≈ 20 kbit s^{-1}.

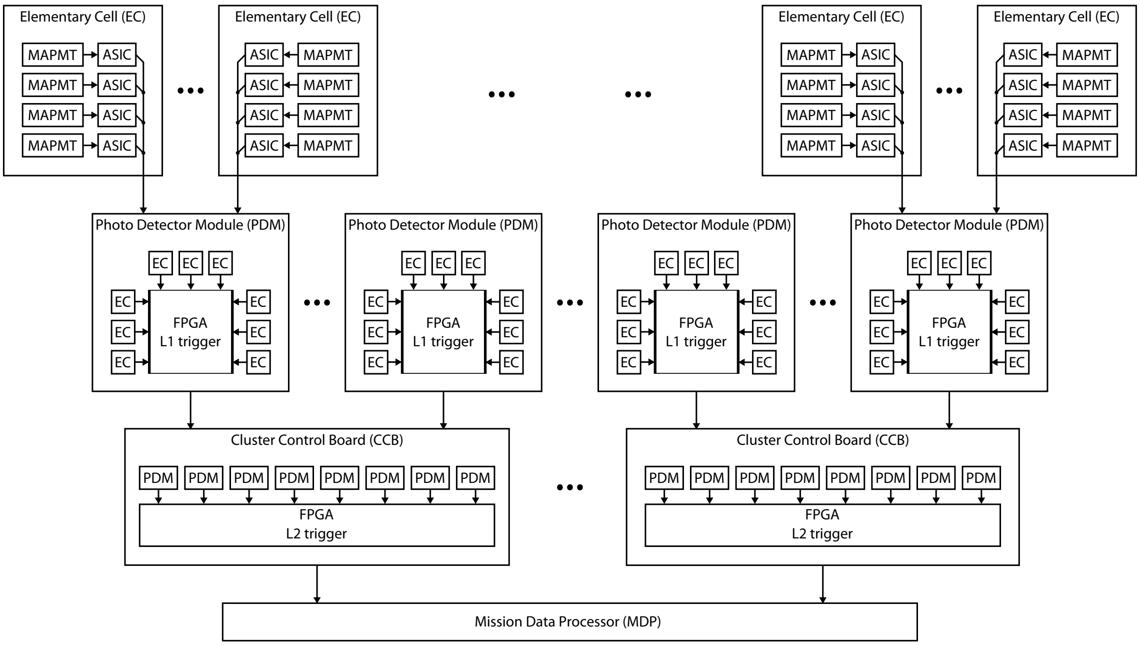

Figure 5.1: Overview of the hierarchical trigger and read-out scheme of the JEM-EUSO detector: Four MAPMTs are grouped together and form the 'EC', of which nine are connected to six PCBs onto which the 36 SPACIROCs are mounted. Together with the PDM control board and its mechanical support frame, this unit is called Photo-Detector Module and represents the basic detector unit. The complete FS of the JEM-EUSO detector is made out of 137 PDMs, and a cluster of 8 to 9 PDMs is read-out and controlled by one CCB. The last level in this hierarchy is the MDP which controls the 18 CCBs. The L1 trigger is implemented at PDM level and the L2 trigger is implemented at the level of the CCB. (Image: Bayer, 2011)

5.1 JEM-EUSO Cluster Control Board

5.1.1 Requirements

The scientific objective – to record the light produced in UHECR induced EASs – sets the minimum amount of time which has to be recorded: the longest duration of such an event is of the order of 150 µs. As the requirement on the timing resolution of the instrument was set to 2.5 µs (the GTU – see also Equation 2.6), it was defined to record 128 GTUs per event, which is around twice the duration needed. This is a compromise which allows to record enough data before and after the event to evaluate the current background, without increasing the event size too much and thus to keep the data rate low. This is especially important as fast and reliable on-board storage (e.g., for the ring buffers on the PDM control board) is a limited and expensive resource.

The primary requirement for the CCB is therefore deduced directly from the L1 trigger rate – or rather, the resulting data rate coming from the PDMs – and from the requirement on the maximum allocated bandwidth for downlink:

- The CCB shall reduce the trigger rate of around 10^3 Hz coming from the PDMs to an output trigger rate lower than 0.1 Hz at the level of the FS.

To handle the large number of 137 PDMs in the current baseline[2], see Figure 2.3) that have to be read out and controlled in parallel by the CCB, the baseline scheme is to divide the FS into clusters of 8 PDMs. The final cluster size is mainly governed by the architecture used to implement the CCB and the available hardware resources. Therefore, a cluster size of 9 PDMs is considered as an advanced option. Additional constraints have to be taken into consideration especially in terms of the allocated mass and power budget and the reliability: a smaller cluster size benefits from a higher degree of inherent redundancy in case of a failing CCB at the expense of higher mass and power demands. This leads to the following requirements:

[1] The CCB has to read out the data generated by a cluster of 8 PDMs (TBD).

[2] The CCB has to be able to handle the data rate associated with an input trigger rate of 56 Hz.

[3] The output trigger rate of the L2 trigger shall be lower than 5 mHz.

As it is not foreseen to have a fixed geometrical relation between the PDMs inside the cluster connected to one CCB, another important requirement for the CCB can be defined:

[4] The data coming from the PDMs shall be processed independently and in parallel.

This requirement on the one hand increases the overall reliability in case of a failing PDM, but on the other hand puts strong constraints on the processing power of the CCB and the architecture used for the implementation.

To maximize the exposure of the experiment, the dead-time of the electronics during which the instrument is ‘blind’ to events has to be minimized as much as possible, without over-constraining the requirements on the detector electronics. Therefore, the maximum allocated processing time is given by the following requirement:

[5] The processing time to evaluate the L2 algorithm has to be less than 100 ms.

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[2] The final amount of PDMs is still To Be Defined (TBD) by the collaboration and depends on the exact shape and size of the FS which in turn is determined by the available launcher (see also Section 2.3.1).

It should be stressed that the dead-time of the instrument, which sets the requirement on the processing time, additionally implies a requirement, that a ‘double buffer’ for the scientific data is implemented on the PDM. This allows to record a second event on the PDM while the previous event is still being processed at the CCB.

Based on the hierarchical design and to reduce the harness of the FS electronics, the MDP has no direct interface to the PDMs. Therefore, the CCB has to control and monitor the PDMs:

[6a] The CCB has to monitor possible failures or anomalies at PDM level.

[6b] Configuration data for the PDM and the FEE have to be provided by the CCB.

[6c] Auxiliary signals for the synchronization of the FS have to be provided by the CCB.

The mechanical structure of the FS foresees to distribute the CCBs onto four dedicated mechanical support structures or boxes, which are mounted inside the four quadrants at the back of the FS. This separation relaxes the constraints put on the thermal structure and will help removing the heat generated by the electronics. The rather large distance, resulting from the routing of the harness, generates a requirement for the main data interface between the CCBs and PDMs:

[7] The interface between CCB and PDMs shall be reliable for routing distances of the harness of up to 3 m.

Finally, general requirements for space electronics regarding low mass and power, as well as reliability in the natural space radiation environment have to be applied, too:

[8a] The total power budget allocated for the CCBs is 13 W.

[8b] The mass and size of the CCB is TBD.

[8c] The CCB shall be radiation tolerant and work reliably in the radiation environment of the ISS orbit.

[8d] The operational temperature range shall be −10 °C to +50 °C and the non-operating temperature range −30 °C to +50 °C.

5.1.2 Implementation

During the first phase of the development of the CCB and after capturing the main requirements, the central technology used to implement the required functionality has to be selected. This is a very fundamental and critical decision and has to be taken very carefully, as a change of the central technology later in the design process is not possible without a complete re-design. This is especially important for the development of electronics for a dynamic project like JEM-EUSO, where functionality is subject to change and central parameters are TBD.

For a data processing hardware like the CCB, the three different technologies which exist today and have to be considered are:

1. MicroController Unit (MCU) or Digital Signal Processor (DSP),
2. Field Programmable Gate Array (FPGA), and
3. Application Specific Integrated Circuit (ASIC).

Each of the technologies has its particular advantages and disadvantages which have to be taken into account and prioritized, and which will be discussed in the following paragraphs.

MCUs are general purpose devices which can be adapted to a particular application by software. Due to their fixed hardware and their optimization to more general functionality like monitoring and controlling, they can be regarded as slow in comparison with data processing or they need to be operated at quite high clocking frequencies, which results in a high power consumption. A DSP overcomes this drawback to some degree by including dedicated hardware or co-processors for commonly used signal processing algorithms. Nevertheless, as these are general purpose devices, MCUs and DSPs are manufactured in high quantities which reduces their costs. In addition, the time needed to develop the application can be kept at a minimum, because code and software for commonly used tasks can be re-used – to some extent even between different architectures and manufacturers.

An ASIC can be placed on the other far end of the spectrum regarding data processing speed, power consumption, costs, and development time. An ASIC is a custom-designed piece of hardware designed for a particular application. They are mainly used to implement analog functionality which has to be implemented externally for MCUs and DSP, but can also contain one or more dedicated and optimized MCUs or special hardware for data processing algorithms. Due to their high degree of optimization for a particular application, they do not contain functionality which is not needed and therefore, the power consumption will be the lowest of the three different technologies while the performance will be the highest. The drawback of this application specific optimization is that ASICs are not flexible at all and any change in the functionality, the requirements, or the parameters will be followed by a re-design of the chip. In addition, because of the generally low quantities produced, the costs are usually very high and the development time is rather long.

The gap between the general purpose MCU and a dedicated ASIC is filled by the FPGA, which can be regarded as an intermediate technology. An FPGA contains an array of logic blocks together with reconfigurable interconnections, and the overall functionality can be programmed after the manufacturing or even changed dynamically during the run-time of the application. Due to the logic blocks, basically any Boolean function can be implemented and is only limited by the size of the array or the available resources. While it is possible to implement a complete MCU inside the FPGA, it should be obvious that in this case, the hardware is not as optimized as a specifically designed MCU. Therefore, the performance will be generally lower and the power consumption higher. Nevertheless, especially since FPGAs offer true parallel processing, high performance data processing algorithms can be implemented such that they can easily outperform a DSPs implementation. While today's FPGAs are not limited anymore to the very basic Boolean logic gates, but also contain special hardware like memories or complete (optimized) microcontroller cores, they usually do not contain analog functionality.[3] In addition, because usually only a certain fraction of the resources available within the FPGA can be used by the application (due to the limited amount of routing or interconnect resources), the power consumption is much higher compared to the one of ASICs. On the other hand, FPGAs are extremely flexible devices, and due to the Hardware Description Language (HDL) – which is the written representation of the circuit to be implemented and allows to some degree to re-use hardware blocks similar to re-using code for an MCU – the development time for an application is usually somewhere between the time needed for MCUs and ASICs. Finally, due to their availability as COTS device, the costs for a single device are low compared to the manufacturing of an ASIC.

An ASIC is well suited for the FEE and the SPACIROC was developed especially for JEM-EUSO (see Section 2.3.3.1). While for the FEE a low power solution was important (nearly 5000 ASICs are used), the main characteristics which drove the technology selection for the CCB was flexibility. The need for a flexible solution was especially important, as the evaluation of a suitable L2 trigger algorithm was still ongoing while the development of the CCB had to be started to stay compliant with the schedule. Finally, due to the need for a high amount of Input/Output (I/O) pins to implement the data and control interfaces for the eight connected PDMs together with the memory interfaces, the selection of the technology was made in favor of an FPGA[4]. In particular, a Xilinx Virtex-4QV FX-140 was selected as a baseline, which was already available as a radiation-tolerant version during that time (with a guaranteed Total Ionizing Dose (TID) of 300 krad(Si) Xilinx, 2010c). As an advanced option, the Xilinx Virtex-5QV FX-130 was selected, which was announced (but not yet available) as a radiation-hard device (guaranteed TID of 700 krad(Si) Xilinx,

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[3] Some FPGAs include a general purpose Analog-to-Digital-Converter (ADC) for basic applications.

[4] A study on available space qualified DSPs had been performed, but the relatively slow and low amount of available General-Purpose Input/Outputs (GPIOs) made the implementation of the data and control interfaces unfeasible.

2010b)[5]. These particular devices were selected because their architecture and the amount of available resources are comparable, which would allow to change to a more modern and more reliable technology during the development of the instrument without a major impact on the schedule. The main benefit of using the Virtex-5QV would be a lower power consumption together with the improved radiation-hardness.

For the prototype board of the CCB developed during this work (see Figure 5.2), a commercially available FPGA was selected in replacement of the space-grade version. In particular, the XC4VFX140-10FFG1517C device was chosen, which contains the same architecture and amount of available Configurable Logic Blocks (CLBs). The lowest speed-grade (10) was selected as this is the only speed-grade available for the space-grade version. One important difference between the space-grade and the commercial-grade version of the Virtex-4 FX140 which has to be taken into account is that the 'RocketIOs'[6] are not supported in the space-grade version. Nevertheless, the corresponding pins are not connected in the device package of the space-grade version and therefore, the two packages are basically pin-compatible. This simplifies the change from the commercial-grade to the space-grade chip in a later design stage, and allows to re-use the layout of the Printed Circuit Board (PCB).

5.1.2.1 Memories

The CCB contains several memories for different purposes, and the appropriate technology which fulfills the different requirements had to be selected and studied. The different memories which have to be implemented are:

- a memory to store the configuration data of the FPGA,
- a memory to buffer the scientific data while the L2 trigger algorithm is evaluated and until the MDP is ready to receive the data,
- and a memory to store intermediate results of the L2 trigger algorithm.

The selected Virtex-4 is a Static Random-Access Memory (SRAM)-based FPGA and thus its configuration is volatile and has to be reprogrammed each time the power supply has been switched off. The requirements on the reliability of the memory that stores this configuration bitstream or firmware are demanding as any bit-flip inside the bitstream could alter the functionality of the FPGA or even render it completely non-functional. On the other hand, the requirement on the speed of this memory is

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[5] The updated version of Xilinx, 2010b – starting from v1.2 – gives a guaranteed TID of >1 Mrad(Si).

[6] The RocketIO Multi-GigaBit Transceivers (MGTs) are a special type of I/O which provide dedicated hardware for the implementation of high-speed serial data-interfaces with data rates up to 6.5 Gbit s^{-1}.

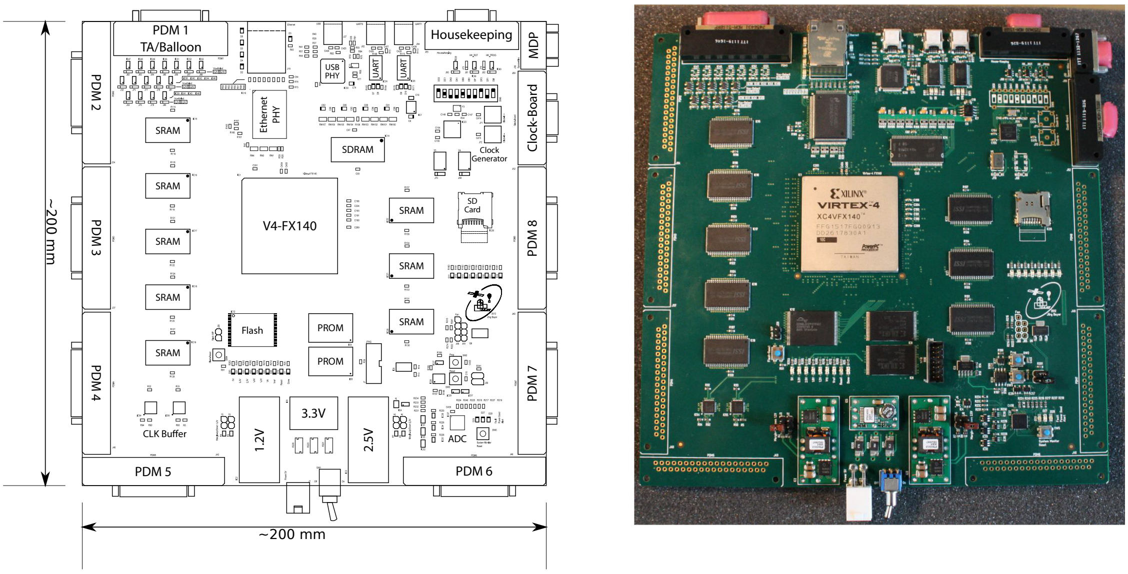

Figure 5.2: A schematic overview (left) of the CCB prototype board for JEM-EUSO and a picture of the assembled board. The most prominent component is the Virtex-4 FX140 FPGA in the center of the board, which is surrounded by the SRAM and the connectors for the interfaces towards the PDMs, the CLKB, the HK, and the MDP. Other components include the power supply (at the bottom) and various interfaces for the development, testing, and debugging (at the top). (Image: Bayer et al., 2013)

not very demanding as this memory is only used after a power cycle and its speed only defines the time it takes to reach the operational state of the CCB.

The Virtex-4 comes with several interfaces to load the firmware bitstream, whereas the two main methods are either to read directly from an external memory attached to a dedicated interface which is controlled by the FPGA itself, or the firmware can be loaded through a dedicated configuration interface which is controlled externally for example by an MCU. Using the latter option, the FPGA could be configured by the MDP, which could read the firmware bitstream from its protected mass-memory which also holds its own software. This would also allow to change the functionality of the CCB during orbit, as a new firmware could be sent from ground to the MDP.

The prototype CCB implements a dedicated Programmable Read-Only Memory (PROM) which holds the firmware of the FPGA and is in-system programmable. In particular, two physically separated memory chips are used – an XCF32P and an XCF16P – which are put into a daisy-chain configuration to hold a total of 48 Mibit[7] of configuration data[8]. The implementation of two physical devices allowed the

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[7] To avoid confusion the binary prefixes according to IEC 60027-2 are used.

[8] The size of the configuration memory of the Virtex-4 FX140 is 45.64 Mibit.

testing of the daisy-chain configuration and the splitting of the firmware bitstream over several devices, which would be the space qualified configuration when using three radiation hard XQR17V16 devices. Another option would be the usage of a single device like the 3DPO64M08VS2299 from 3D Plus connected to the same interface.

The buffering of the scientific data is less demanding with respect to radiation hardness (as the time during which the data have to be stored is only of the order of 100 ms), but puts strong requirements on the speed of the memory. The required data rate can be estimated from the data packet size[9] of 20.53 Mibit and the requirement of the input trigger rate coming from the connected PDMs of 56 Hz, which results in around 1.14 Gibit s^{-1}. While the Random-Access Memory (RAM) available inside the FPGA could easily handle the data rate, the total available amount[10] is only 8.625 Mibit and therefore not large enough to store a complete data set. On the other hand, an external, space qualified memory which is large enough can be easily found, but the access times are rather slow and therefore, the data bus width has to be large enough to comply with the high data rate. Therefore, and to fulfill the requirement on the independent and parallel processing of the connected PDMs, one physical memory is implemented for each PDM. As a baseline, the HX6408 memory from Honeywell was selected, which is a radiation hardened SRAM with a total of 4 Mibit organized as $512\text{k} \times 8$ bit and provides fast access times (20 ns to 25 ns depending on the total dose hardness) together with a low power consumption (260 mA during write access at 40 MHz). As an industrial grade replacement for the prototype board, the IS61WV5128BLS-25TLI was selected, which is comparable in terms of its timing, its power requirements, and is also pin-compatible.[11] With a memory access time of 25 ns, a data rate of 320 Mbit s^{-1} per PDM is achieved, which is twice the requirement and reduces the overall dead-time of the instrument.

At the time of the component selection process for the CCB, space qualified Dynamic Random-Access Memory (DRAM) was just becoming available. DRAMs offer higher storage densities, but have in general a higher power consumption and slower access times due to the memory refresh cycles, which are needed to prevent data loss. To test the technology and to provide a high amount of storage as an advanced option, which can be used to record slow events like meteors or TLEs, a Double Data

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[9] Assuming one packet of 128 GTUs of photon counting and KI data from the triggering PDM cluster without any engineering data: 8 PDMs × 9 ECs × 4 MAPMTs × (64+9) Channels × 8 bit × 128 GTUs ≈ 20.53 Mibit.

[10] Not including the parity bits which can be used to implement an Error Correcting Code (ECC).

[11] When the prototype board was assembled, the slower version of this SRAM was not available on the market. Therefore, it was replaced by the faster IS61WV5128BLL-10TLI, but still the slower timings of the HX6408 are used to access the memory. A minor difference in the order of the data bits is present, which has no impact on the operation.

Rate-Synchronous Dynamic Random-Access Memory (DDR-SDRAM) is additionally available on the prototype board. Two MT46V32M16P chips are implemented and addressed in parallel to provide a 32 bit wide data bus running at a maximum of 200 MHz. This configuration provides a total of 1 Gibit storage[12] with a maximum peak transfer rate of 12.8 Gbit s^{-1}.

The Virtex-4 FX140 includes two embedded PowerPC 405 (PPC405) MCUs, which could be used for high-level control and monitor tasks. But as these MCUs are not available in the radiation hard version of the Virtex-5, this is not considered as a baseline option – nevertheless, the implementation of a small MCU as a softcore like the PicoBlaze is still an option for the Virtex-5. To study this possibility, the prototype CCB also provides a non-volatile memory for the storage of the code. This storage is implemented with the S29GL512P11TFI020 chip, providing a total of 512 Mibit of flash memory on a 16 bit wide data bus.[13]

5.1.2.2 Interfaces

With regard to the data flow, the CCB is located between the PDMs and the MDP and therefore, the interfaces towards these devices are the main data interfaces and considered critical. To provide reliable and fast data transfer over the rather large distance of up to 3 m (see Section 5.1.1), the Low-Voltage Differential Signaling (LVDS) standard was selected as physical layer for all interfaces. As the name suggests, LVDS is a differential signaling standard which uses a pair of wires (or PCB traces) to transfer information. A constant current is sent through one wire and returning through the other, whereas the actual bit information is carried by the direction of the current. A termination resistor close to the receiver through which the current flows generates a voltage drop, which is measured by a differential amplifier to determine the polarity and therefore the logic level. By tightly coupling the electric- and magnetic-field of the two wires, LVDS is not susceptible to external electromagnetic noise and at the same time keeps the generated electromagnetic noise at a minimum. In addition, the termination resistor can be matched to the impedance of the wires preventing signal reflections, thus reducing the noise at the receiver. This allows to transfer data at high speed over large distances with low power consumption due to the low voltage levels involved. Both selected FPGA devices already contain hardware macros (I/O drivers/receivers) that provide support for the LVDS standard. Therefore, additional external driver/receiver chips are not necessary. This simplifies the board layout but at the same time increases the number of required I/Os from

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[12] The layout of the board also provides support for the MT46V64M16 chip, thus supporting a maximum of 2 Gibit.

[13] As all 26 address lines are routed in the layout, the amount of storage could be easily increased to 1 Gibit by assembling an S29GL01P chip.

the FPGA.

As it can be seen from the schematic overview of the layout in Figure 5.2, the size of the board is basically given by the large amount of connectors needed for the interfaces – especially for the connectors to the PDMs. This could be improved by using stacked connectors (which are available) or by attaching the connectors via wires to the board, which would allow to mount the connectors on one or more sides of the mechanical support structure. This concept was implemented in the CCB for EUSO-Balloon and EUSO-SPB (see Section 5.2).

PDM The main interface between CCB and PDM to transfer the scientific data has big impact on the overall performance of the detector as the transfer time adds to the dead-time of the instrument. Furthermore, the interface additionally influences the general architecture of the CCB as buffers, external memories, and the L2 trigger implementation have to be compliant with the data rate. In general, a trade-off has to be found between the number of data channels used, which is constrained by the available I/Os, and the single channel speed, which is constrained by the chosen technology (i.e., the FPGA and the harness including connectors). A possible solution was developed and studied in Bayer, 2011 and successfully tested with a data rate of up to $12.8\,\mathrm{Gbit\,s^{-1}}$.

This solution was regarded as too sophisticated to be implemented in the PDM control board at that time, and a simple parallel interface was realized. This unidirectional and source-synchronous interface runs at 40 MHz on 8 data channels to transfer one byte per clock cycle and thus achieves a data rate of $320\,\mathrm{Mbit\,s^{-1}}$. Despite the fact that this is much slower[14], the data rate is still compliant with the expected trigger rate of 56 Hz, resulting in a mean data rate of around $150\,\mathrm{Mbit\,s^{-1}}$.

To monitor the status and to read and write the configuration parameters of the PDM, an additional Serial Peripheral Interface (SPI) is implemented. This interface runs at 2 MHz with 32 bit words, which provides a large enough address space especially for the huge amount of configuration parameters for the SPACIROCs.

Finally, a few dedicated signals for synchronization and timing have been implemented:

- An L1 trigger input coming from the PDM used to start the data transfer.
- An external trigger output used to stop the ring buffer on the PDM and to read out the data if an adjacent PDM from the same cluster issued an L1 trigger. This signal is also used as an external trigger or to read out the data by telecommand.

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[14] This data rate could have been easily achieved with one single data channel from the interface proposed in Bayer, 2011, thus reducing the connector and harness size.

- A system clock output, which is the main clock for the PDM and the SPACIROC. This clock is provided by the CLKB at a frequency of 40 MHz and distributed by the CCB.
- An output of the central GTU clock at a frequency of 400 kHz also provided by the CLKB.

To minimize the space needed by the interface, a Micro-D connector is used which is available in space grade versions of different sizes. In particular, the 37 pin model is used for the interface with the PDM, which provides enough pins to implement the various interfaces and even allows one additional spare LVDS pair.

To simplify the development and to have the possibility to implement additional signals during the integration of the prototype instrument, one PDM interface was replaced by a model with 51 pins. This gave the possibility to realize a total of 8 spare LVDS pairs, but due to the limited amount of available I/Os, it was necessary to use external LVDS drivers/receivers. This special connector is labeled with ‘PDM 1 TA/Balloon’ in Figure 5.2, and it was foreseen to keep the 51 pin option for the EUSO-Balloon.

MDP The decision on the interface between CCB and MDP was taken in favor of the SpaceWire standard, which is a spacecraft communication network specified by ESA and widely used on various space missions. This standard is defined in ECSS-E-ST-50-12C and allows fast[15] full duplex communication. By implementing a commonly used and properly defined standard with available COTS hardware, the time needed for the development and especially the integration of the interface could be kept low. Complying with the standard, a Micro-D 9 pin connector is mounted on the CCB and the SpaceWire interface is running at a nominal speed of 200 Mbit s^{-1}, which is the maximum data rate supported by the MDP hardware.

CLKB The interface with the CLKB implements various signals which are necessary to synchronize the instrument and provide information on the performance of the detector like the measurement of the operational- and dead-time:

- an L2 trigger output from the CCB to measure the performance;

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[15] The standard does not fix the maximum data rate, only a lower limit of 2 Mbit s^{-1} is defined which is based on the timeout to detect a disconnected link. Therefore, every system needs to define its own maximum data rate, which depends on the particular implementation and technology used or the cable length, and needs to be evaluated based on the signal jitter and skew. It is even allowed to use different data rates for both directions within the same link. Nevertheless, most hardware implementations support up to 200 Mbit s^{-1}, but recent hardware can be found which supports up to 400 Mbit s^{-1}.

- an external trigger input from the CLKB, which is used to implement different operational modes and to read-out the data via telecommand;
- a busy signal input indicating that the MDP is not ready to receive the data;
- a time-sync pulse input used to generate accurate time stamps for the data packets and the triggers;
- a system clock input (40 MHz), which is used by the CCB as base clock to generate various system and interface clocks and is also routed to the PDM;
- an input of the central GTU clock (400 kHz) used to generate time stamps and routed to the PDM.

The signals are routed to a Micro-D 15 pin connector, which also provides additional signals for shielding to increase the signal quality especially for the system clock.

HK An SPI running at 2 MHz and configured for 32 bit words has been selected to transfer the engineering data from the CCB to the central HK board, which collects all the housekeeping data from the instrument. In addition, a few dedicated signals were implemented:

- An alarm interrupt to the HK can be issued by the CCB if any monitored parameter gets out of the defined operational range, so that the HK can react immediately. This signal is also used in case the CCB detects an abnormal condition on the PDM.
- An additional alarm output is provided, which indicates that an error occurred while loading the firmware of the FPGA.
- A ‘soft’ reset input, which resets the internal logic of the FPGA.
- A ‘hard’ reset, which re-loads the firmware of the FPGA.

All signals are implemented on a Micro-D 15 pin connector.

5.1.2.3 Clocking Resources

The main clocking source for the CCB is the CLKB, which provides a 40 MHz system clock and the GTU clock at a frequency of 400 kHz. Both clocks are fed into a programmable, low skew clock driver (ADN4670), which provides 10 LVDS outputs and is used to distribute the clocks to the connected PDMs and the CCB. The outputs of the clock driver can be enabled/disabled via a simple serial programming interface and thus the clock outputs for not connected PDMs can be disabled in order to reduce the power consumption and the generated electromagnetic noise.

During the development and evaluation of the firmware of the FPGA, it is not feasible to always operate the CCB with the CLKB connected. In addition, some hardware of the FPGA is depending on a low jitter clock source at higher frequency – this would be the case for example if a fast serial interface will be implemented (see Bayer, 2011, Section 4.2). Therefore, additional clocking resources are available on the prototype CCB, which are removed for the flight hardware.

The layout includes two footprints onto which standard oscillators can be mounted. As the layout supports differential and single-ended oscillators with a supply voltage of either 2.5 V or 3.3 V (which can be altered via a solder jumper), a huge range of oscillators with different frequencies is available. In the current configuration of the CCB, one footprint is populated with a low jitter 200 MHz LVDS oscillator, which is used to generate different internal system clocks. The other footprint is left unpopulated, in order to mount an additional oscillator if needed.

Finally, a very versatile and flexible clock resource is available with the MAX3638 Integrated Circuit (IC). This programmable Phase-Locked Loop (PLL) clock generator provides a total of nine outputs (out of which 3 are routed to the FPGA) with programmable dividers. Together with two available input clocks (a 25 MHz crystal and connectors for an external clock generator), the outputs can be operated over a wide range of frequencies. Programming of the clock generator and its internal dividers is done with switches available on the board. The main purpose of this clock generator is to have the possibility to easily test the performance of the FPGA firmware and its timing at different frequencies. In addition, it can be used to generate up to three different synchronous clocks, which is necessary to evaluate the performance of the DDR-SDRAM in conjunction with the PPC405 cores.

5.1.2.4 System Monitor

As the Virtex-4 FPGA does not contain an ADC[16] to monitor the various supply voltages or the internal temperature of the FPGA, an external ADC is implemented. To have the possibility to monitor the system even in case of a problem at the level of the FPGA, a power-supply monitor (MAX34441) was implemented which can monitor up to five voltage rails and several temperature sensors. The parameters of the system monitor (such as over-/under-voltage thresholds) are programmed via an industry standard 2-wire serial bus (I^2C), and it can automatically generate an alarm in case one of the monitored parameters is out of range. The MAX34441 is connected simultaneously to the FPGA and an USB transceiver IC (FT2232) in order

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[16] While the Virtex-5 contains an ADC and the 'system monitor', the support was removed for the Virtex-4 in early datasheet versions.

to either provide the engineering data to the HK board via the FPGA, or to read the present voltages, currents, and temperatures with an external computer during the development.

The system monitor is able to monitor the voltage of all five power supply rails (see Section 5.1.2.6) with the help of simple resistive voltage dividers in order to keep them within the full scale input voltage specification of the ADC. In addition, the currents of the three main voltage rails (i.e., 1.2 V, 2.5 V and 3.3 V) are measured via the amplified voltage drop across a sense resistor. Due to the fact, that the ADC, or its input Multiplexer (MUX), has only 6 available channels, each of the voltages and currents of the above mentioned rails are fed into a Single Pole Double Throw (SPDT) analog switch, which is controlled by the system monitor in order to read the values one after the other (this implements an additional multiplexer stage).

Besides the voltages and currents, the system monitor can also measure its internal temperature and the core temperature of the FPGA via a temperature-sensing diode (diode-connected transistor). A software was written to display and log all the data from the system monitor during the development and the integration process. This software is also used to setup the operational data of the system monitor, like the calibration parameters of the ADC or the alarm thresholds.

5.1.2.5 Development Hardware

To simplify the development and debugging process and to increase the possibilities to test the FPGA configuration, additional hardware has been implemented on the prototype CCB. This includes LEDs to display internal states, two USB to Universal Asynchronous Receiver Transmitter (UART) ICs for low-speed data transfer and as a command interface, one high-speed USB IC which is also directly connected to the system monitor in order to read the engineering data independently from the FPGA, one tri-mode Ethernet Physical Layer (PHY) supporting Gigabit Ethernet for fast data transfer, and a socket in which an industry standard Secure Digital (SD) memory card can be fitted to have access to a large non-volatile flash memory.

These additional hardware will be removed in the final flight hardware version, which will allow to support an additional PDM as an advanced option (nine in total).

5.1.2.6 Power Supply

To design the power supply of the CCB, the different power requirements have to be defined. While the definition of the necessary voltage rails and the corresponding voltage requirements is a straight forward task, the definition of the power (current) requirements is not obvious. Most ICs like MCUs are designed for a specific task and thus their power supply demands are fixed within a certain range and can be found in the datasheet from the manufacturer. This is in contrast to FPGAs, which can implement basically any functionality at a wide range of frequencies which is not even fixed at the end of the design cycle. Therefore, the power supply design has to start with a conservative worst case design and undergo an iterative redesign as the functionality of the FPGA is finalized. This is especially important for the design of the decoupling network, as the transient current demands are unknown but causing power supply noise and ground bounce. The manufacturer of the FPGA (Xilinx) provides with the XPower Estimator (XPE) a tool to estimate the power consumption of the design which can be invoked at any stage of the design process. It should be obvious that the tool can only provide an accurate estimate if the input data are close to the final design. This tool was used for a first estimate on the power consumption of the FPGA with estimates on the amount of logic that will be used, together with the planned internal clock frequencies and amount of switching I/Os. Together with the power requirements from the peripheral hardware, a first power supply system was implemented.

The CCB contains a total of five different voltage rails, which are generated from the 5 V input supplied by the LVPS:

1.2 V This is the main internal supply voltage for the FPGA and has thus the highest degree of uncertainty. The estimated power consumption from the XPE gave around 1.8 A, of which nearly one half can be accounted for the quiescence current of the FPGA. Due to the high degree of uncertainty, a margin of 50 % was added, which leads to a maximum power consumption during operation of 2.7 A. In addition, the worst case power-on requirement given in the datasheet for this voltage rail is 4.25 A. Therefore, a high efficiency point-of-load switching regulator (PTH05010W) was selected which has its peak in efficiency (more than 90 %) between 3 A and 6 A and can deliver up to 15 A. This should include enough margin to also evaluate the two embedded MCUs as advanced option, whose power consumption is not included in the XPE estimate. As the output voltage tolerance is better than ±2 % it meets the requirement of the FPGA, which is ±5 %. To easily test the performance of the FPGA over its allowed supply voltage range, the output voltage can be adjusted by ±5 % with simple jumpers.

2.5 V This is the main I/O supply rail and it is powering all the LVDS drivers inside the FPGA as well as the external drivers for one PDM interface (see 5.1.2.2). In addition, it is also powering the eight external SRAMs and thus also the I/O drivers for the memory interfaces. Using the estimate from the XPE for the auxiliary power consumption of the FPGA and adding an estimate for the power consumption of the external memories and their interfaces, the conservative estimate on the total power requirement from the 2.5 V rail is around 3 A, including a margin of 50 %. As this is similar to the 1.2 V requirement, the same regulator (PTH05010W) was chosen.

For the evaluation of the DDR-SDRAM as an advanced option, the 2.5 V rail will also power this memory and its interface. To increase the efficiency, two more voltage rails are generated out of the 2.5 V: the termination voltage for the DDR-SDRAM interface (see 1.25 V) and the 1.8 V, for which the regulator should provide enough margin.

3.3 V This voltage rail is needed for the interface of the configuration PROM, the clock generator and the additional debugging/development hardware like the USB IC, the Ethernet PHY, and Flash memories. Adding up the maximum power consumptions from the datasheets of the ICs, a total power requirement of around 1 A can be found (including 25 % margin). Therefore, a power regulator with peak efficiency around 1 A was chosen (PTH0400W) which can output up to 3 A.

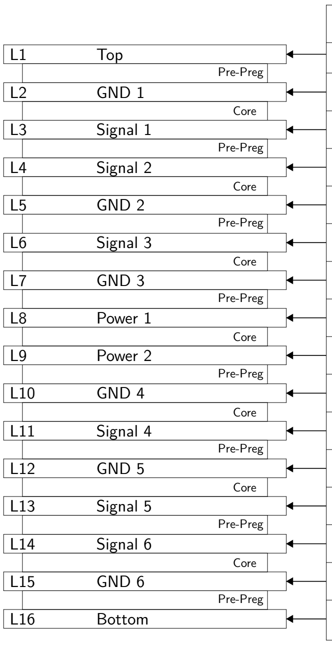
1.8 V The PROMs need an additional core supply voltage with a requirement of only 10 mA, as both PROMs are never active at the same time due to the daisy-chain configuration. In addition, the 1.8 V is also used by the Ethernet PHY, which has a power consumption of 430 mA. As the Ethernet PHY is only active while testing and to simplify the layout, a small linear regulator (TPS72501) was chosen with a maximum output current of 1 A, which is supplied by the 2.5 V rail.

1.25 V The interface between the FPGA and the DDR-SDRAM is implemented with Stub Series Terminated Logic (SSTL), which uses an active termination scheme to reduce signal reflections associated with high-speed interfaces. This termination scheme uses a serial resistor at the source (the on-chip termination of the FPGA is used) and a parallel resistor at the receiver side, tied to the termination voltage which is exactly half of the memory supply rail. This termination voltage has to source and sink currents up to 3 A and is generated by a dedicated linear regulator (LP2995) powered from the 2.5 V rail.

To ensure the proper start-up and configuration of the FPGA, a specific power-on sequence of the different voltage rails is required. To fulfill this requirement, the ramping up of the power rails is synchronized, which ensures that the 1.2 V core voltage is the first powered up, followed by the 2.5 V auxiliary voltage and the I/O voltages. In addition, a voltage supervisory circuit delays the FPGA configuration until all voltage rails are within their specifications, or resets the FPGA if any voltage rail is out of specification.

5.1.3 Printed Circuit Board Layout

The layout of the CCB is mainly driven by the FPGA and the routing of the signals between the FPGA I/Os and the memories or interfaces (62 I/Os per PDM). As shown



Single-Ended				Differential		
Copper	Model	Target Impedance	Trace Width	Model	Target Impedance	Trace Width/Separation
18 µm	Coated Microstrip	50 Ω	100 µm	Edge-coupled Coated Microstrip	100 Ω	100 µm/150 µm
18 µm						
18 µm	Offset Stripline	50 Ω	200 µm	Broadside-coupled Stripline		100 µm/-
18 µm	Offset Stripline	50 Ω	200 µm	Broadside-coupled Stripline	100 Ω	100 µm/-
18 µm						
18 µm	Stripline	50 Ω	125 µm	Edge-coupled Stripline	100 Ω	100 µm/150 µm
18 µm						
35 µm						
35 µm						
18 µm						
18 µm	Stripline	50 Ω	125 µm	Edge-coupled Stripline	100 Ω	100 µm/150 µm
18 µm						
18 µm	Offset Stripline	50 Ω	200 µm	Broadside-coupled Stripline	100 Ω	100 µm/-
18 µm	Offset Stripline	50 Ω	200 µm	Broadside-coupled Stripline	100 Ω	100 µm/-
18 µm						
18 µm	Coated Microstrip	50 Ω	100 µm	Edge-coupled Coated Microstrip	100 Ω	100 µm/150 µm

Figure 5.3: The stackup (cross section) of the JEM-EUSO prototype CCB as it was provided to the manufacturer. A total of 16 copper layers are used, out of which 8 layers are dedicated to the routing of the signals for the different interfaces. To improve the signal integrity and the power distribution network, several ground planes were implemented together with two thicker planes in the middle of the stackup, which carry the power of the main voltage rails. Also given in the table are the design parameters, which were applied to reach the target impedance of the single-ended and differential signals. These parameters were slightly adjusted by the manufacturer according to the tolerances of the production process, which is common practice (see also Section 6.1).

in Figure 5.2, the FPGA is placed roughly in the center in order to have access to all I/O pins and to keep the number of required routing layers low. The minimum amount of signal routing layers is foremost defined by the properties of the Ball Grid Array (BGA) from the chip and the technology used to manufacture the PCB.

The Virtex-4 FX140 is available in an FFG1517 flip-chip package which has a matrix of 39 × 39 pins (BGA) at a pitch of 1 mm. By applying the recommended PCB design rules from Xilinx, 2006, the diameter of the escape via land[17] is 0.61 mm, which leaves a routing channel width of 0.39 mm between the vias. This allows only one signal to be routed between the vias when the smallest structures are

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[17] Due to the small pitch of the BGA, it is not feasible to route all signals on a single layer. Fan-out or escape vias are used to route the balls to different layers in order to fan out and access all BGA pins.

≥125 µm, or two signals when reducing the structures to ≥75 µm. As the 125 µm design structures was the industry standard at that time, the additional costs for 75 µm structures were much higher than a few additional board layers. Therefore, and due to additional requirements resulting from the impedance matching (see below), design structures of 100 µm have been selected. By having one signal per routing channel between the vias, only one BGA row can be routed per inner PCB layer and two rows on the first and second layer, which defines a minimum amount of signal layers.

Additionally, the impedance of the PCB wires is controlled to improve the signal quality by reducing reflections which can occur due to impedance mismatch between the driver/receiver and the wire. This is especially important for the LVDS signals and the fast data interfaces for the memories and the Ethernet PHY. To control the impedance of the signals, a variety of different trace geometries can be implemented, which are depending on the routing layer inside the PCB stack – e.g., the wire or trace can be routed on an internal layer or on an outer layer – and on the signaling standard, which can be single-ended or differential. The geometrical properties of the trace – like the width of the trace, the distance to the electrical reference or return path, or the distance between two traces in a differential configuration – together with the permittivity (or relative dielectric constant) ϵ_r of the insulator defines its impedance. The characteristic impedance can then be approximated with available models.

Implemented on the CCB are the following structures with a target impedance of 50 Ω for single-ended signals and a target differential impedance of 100 Ω for differential signals (see also Figure 5.3):

- Microstrip: For single-ended signals on the top and bottom layer (or coated microstrip as the traces are covered by the solder-stop mask).
- Edge-Coupled Microstrip: For differential signals on the outer and inner layers (or coated edge-coupled microstrip as the traces are covered by the solder-stop mask).
- Stripline and offset stripline: For single-ended signals on internal layers.
- Broad-side coupled stripline: For differential signals on internal layers.

The decision to use two internal layers to route the LVDS signals in a broad-side coupled stripline configuration was taken to simplify the routing of the differential pairs. In this configuration, the signals are placed on top of each other, and the distance between them (which influences the impedance) is controlled by the manufacturing process or the thickness of the laminate between the two layers. Thus, the impedance can be easily adjusted without major impact on the layout itself.

Using an edge-coupled stripline configuration would mean that the exact distance between the differential pair needs to be controlled during the design process, which was not automatically supported by the employed layout software. The measurements on the final impedances are given in Table 6.1.

Another critical parameter in the layout of the board is the length matching of the routed signals. To ensure signal integrity and to benefit from the noise immunity of the differential signaling, the length between the two signals within one differential pair have to be matched as close as possible – otherwise, any induced noise on the signals would not perfectly cancel out. Additionally, the overall length of the various signals which are part of one particular interface have to be matched within a certain range to ensure the proper timing of the interface. This does especially apply to the large parallel interfaces like the data- and address-buses of the memories. For example, to sample the correct address or data, the bits basically have to be available at the same time or within the timing requirements, which get tighter as the speed of the interface increases. Therefore, the most stringent requirements were applied to the routing of the fast interfaces like the DDR-SDRAM (effectively running at 400 MHz), the SpaceWire interface (designed to run up to 400 MHz), and the Gigabit Media Independent Interface (GMII) towards the Ethernet PHY (running at 125 MHz).

5.2 EUSO-Balloon & EUSO-SPB Cluster Control Board

The main objective of the EUSO-Balloon flight was devoted to the demonstration of the technology developed for JEM-EUSO and to raise the TRL of the key components (see Section 3.2). Therefore, the hardware developed for EUSO-Balloon should resemble the JEM-EUSO hardware as close as possible. On the other hand, especially because only one PDM is used to demonstrate the detection principle, there is no need for a large and complex CCB which could handle 8 PDMs. Thus, it was decided to develop a smaller version of the CCB capable of handling one PDM which is dedicated for EUSO-Balloon, EUSO-SPB and EUSO-TA.

5.2.1 Implementation

Due to the required technological similarity with respect to the JEM-EUSO hardware, most of the requirements given in Section 5.1.1 also apply to the small version of the CCB. In addition, most of the selected components are the same in order to keep the given road-map towards space qualified hardware valid.

Nevertheless, to reduce the power requirements of the CCB, a smaller version of the FPGA was selected. In particular, the XC4VFX60-10FFG1152I was chosen, which provides less logic resources but as it is from the same family, it contains the same

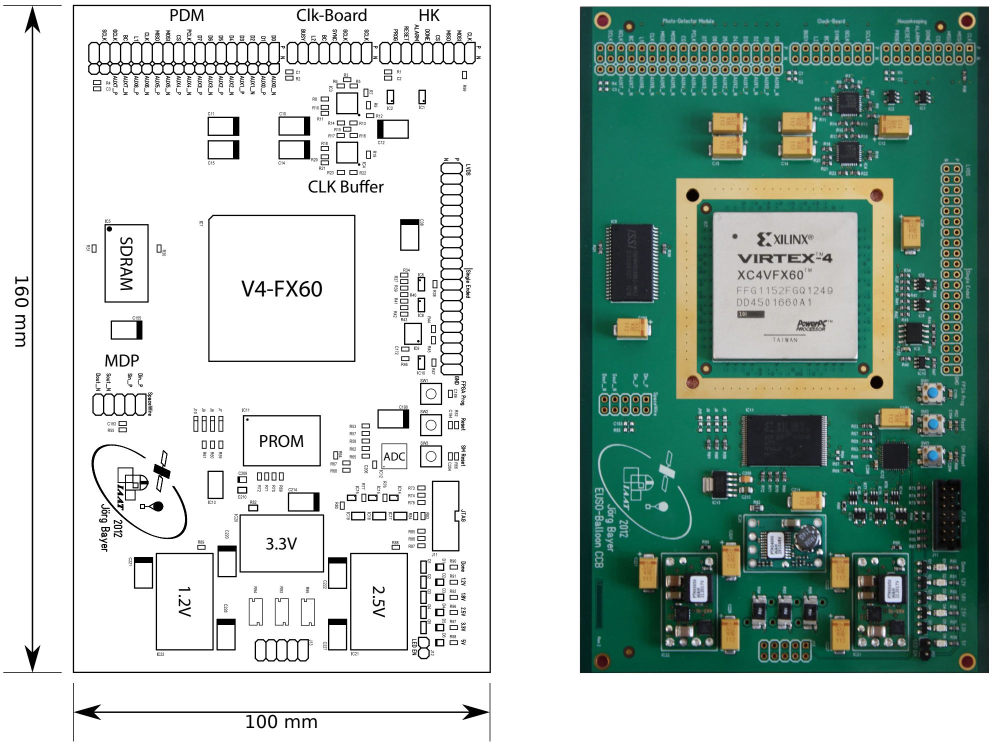

Figure 5.4: Schematic overview (left) and the assembled PCB (right) of the CCB which was developed for the EUSO-Balloon and the EUSO-SPB project. The FPGA, which is the central component of the CCB, is clearly visible in the middle of the board, surrounded by a golden structure, which is an integral part of the thermal structure (see Section 5.2.2). The pads visible above the FPGA are the soldering points for the connectors as they are not mounted directly to the board in order to save space. The SRAM to buffer the scientific data is mounted to the left of the FPGA, and the PROM, which holds the firmware bitstream, is visible below. The lowermost quarter of the PCB is dedicated to the power supply and the system monitor. (Left image based on: Bayer et al., 2013)

technology and architecture as the space qualified version.

A schematic overview of the balloon CCB and a picture of the assembled board is given in Figure 5.4. As it can be seen, the board is much smaller compared to the JEM-EUSO version, and the implemented periphery is reduced to its bare minimum to simplify the layout and reduce the size of the board. As data from only one PDM have to be processed, just one SRAM chip was kept and additional memories like the DDR-SDRAM or the flash were removed. Due to the smaller size of the FPGA, which results in a smaller configuration memory, the firmware bitstream fits into one PROM (XCF32P) and thus the second chip and the daisy-chain configuration could be omitted.

The only available clocking resource is the one provided by the CLKB, and additional oscillators or the PLL are not implemented. To validate the synchronization scheme of the instrument, together with the distribution of the clocks via the CCB towards the PDMs and the ASICs, the low-skew clock driver (ADN4670) is kept, and outputs which are not needed are switched off by default. Nevertheless, to thoroughly test the clock distribution system, all outputs are properly terminated and can be activated. By that, it is for example possible to quantify the amount and impact on the overall jitter when all outputs are activated and driving a load.

The system monitor, which collects data on the different voltages, currents, and temperatures to provide them to the HK system, shares basically the same implementation. Due to the missing DDR-SDRAM and its termination voltage, one channel of the ADC became free, which was then used to monitor the main 5 V input provided by the LVPS system.

Due to the lower power consumption – a consequence of the smaller FPGA and the omitted periphery – the power supply was slightly adapted to the new requirements. Keeping the same technology as for the JEM-EUSO prototype CCB, the point-of-load switching regulators for the 1.2 V and 2.5 V power rails were replaced by smaller versions from the same family with lower output capabilities. In particular, the PTH05050W was implemented, which can provide a maximum output current of 6 A with a peak in efficiency around 3 A (approximately 87 % at 1.2 V and 93 % at 2.5 V output voltage). The voltage converters for the 3.3 V and 1.8 V rails, the power supply supervisory circuit, and the power-on sequence management are not changed. Regarding the implementation of the thermal structure, the utilization of high-efficiency power converters was especially important, in order to comply with the thermal requirements of the balloon flights and the associated low-pressure environment (see Section 5.2.2).

As already mentioned, additional periphery for the development and debugging process had been removed, and only a pin header which provides access to a total of 10 single-ended and 10 differential GPIOs had been implemented in the layout. These GPIOs can be connected to a logic analyzer during the development, or serve as spare signals.[18]

From the system architecture point of view, the balloon CCB is part of the DP and is integrated in the same mechanical support structure – together with the CPU, the CLKB, the GPS, the HK, and the LVPS (see also Figure 3.4 and 3.5). The mechanical structure for the DP is made out of a COTS 19 inch rack with a height of 6 U, which

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[18] After the first prototype boards were integrated for EUSO-TA, the interface between the CLKB and the CCB was improved to simplify the measurement of the dead- and life-times of the instrument, and several additional signals were implemented. The new interface makes use of the spare GPIOs and therefore, a redesign of the board could be circumvented.

contains a sub-rack divider for 3 U units[19]. This sets a requirement on the size of the PCB in order to fit into the sub-rack, which is 100 mm × 160 mm. In order to satisfy this requirement, the connectors are not mounted directly to the board, instead they are connected via cables, which allows to mount them in two rows on the front panel. All in all, it is possible to mount the CCB inside a 3 U frame with 10 HP in width[20] (the size of the front panel is 128.5 mm × 50.5 mm).

5.2.2 Thermal structure

Due to the low-pressure environment during the balloon flights (around 3 mbar), the heat generated by the electronics can only be removed from the instrument by radiation, because convection is not effective anymore. Therefore, the thermal architecture of the CCB plays a critical role, and because its design is deeply connected with the layout of the board and the mechanical structure, it had to be taken into account already during the early planning and design phases.

A thermal analysis of the instrument under various possible flight scenarios and their resulting different operational conditions has been performed (Medina-Tanco et al., 2012).[21] The main purpose of this study was to show, that the mechanical architecture of the instrument can keep the electronics at a temperature, which guarantees their safe operation for the extreme hot and extreme cold scenario. This analysis showed that the skin temperature of the electronic boxes inside the instrument booth can be controlled to stay between −20 °C and +50 °C by adjusting the Styrofoam coverage factor of the main radiator on top of the instrument (see Figure 3.2). This study directly sets the requirement on the operational temperature range for the electronics inside the instrument booth. A similar thermal simulation had also been performed for EUSO-SPB. Based on a fixed launch site and season, together with updated data gathered during the EUSO-Balloon flight, the requirement was slightly relaxed and thus the thermal structure designed for EUSO-Balloon was also valid for the EUSO-SPB flight.

To ensure that the system will meet the thermal requirements not only imposed by the flight but also by transportation and storage, a thermal test procedure was developed (see Medina-Tanco, 2012), which is outlined in the following:

1. identification of risky internal components which could reach temperatures outside their operational range;

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[19] One rack unit (U) is $1\frac{3}{4}$ inch = 44.45 mm.

[20] One horizontal pitch (HP) unit is $\frac{1}{5}$ inch = 5.08 mm.

[21] This included different launch sites and dates, for example Kiruna, Sweden, in winter for the cold case (with a ground temperature of −30 °C, a ceiling temperature of −100 °C and a minimum IR flux of 70 W m^{-2}) and Alice Springs, Australia, in summer for the hot case (with a ground temperature of 10 °C, a ceiling temperature of 0 °C and a minimum IR flux of 340 W m^{-2}).

2. for each risky component, a solution has to be found and implemented;
3. to validate the found solution, the subsystem needs to be turned on under a representative load equal to its operating conditions and temperature cycled between −20 °C and +50 °C at 3 mbar (to ensure that convection is basically eliminated).

All electronic components of the CCB were selected to comply at least to the industrial temperature grade, which means an operational temperature range from −40 °C to +85 °C. This immediately fulfills the low temperature requirement, and the requirement on the maximal thermal resistance between the component on the CCB and the radiator can be calculated with its estimated power dissipation. The following list gives an overview on the components with the highest power dissipation, which was calculated either by the values given in the respective manufacturer datasheet, or directly derived from measurements on the balloon prototype CCB which was operated in the framework of the EUSO-TA project (e.g., for the FPGA). Components with a power dissipation below 100 mW were not considered critical.

XC4VFX60-10FFG1152I The Virtex-4 FX60 FPGA in the industrial grade version has a operational junction temperature T_J range of −40 °C to +100 °C. As the central component on the CCB, it dissipates the vast majority of the total power, which is measured to be around 4 W under full load. Therefore, the total thermal resistance between the FPGA junction and the main radiator for the electronics has to be lower than $R_\theta = 12.5\,\mathrm{K\,W^{-1}}$.

2.5 V PTH05050W The regulator for the 2.5 V power rail has a total input power of $P_{in} = 4.2\,\mathrm{W}$. With an efficiency of 90 %, the regulator has to dissipate around 420 mW, which means the total thermal resistance must be less then $R_\theta = 87.5\,\mathrm{K\,W^{-1}}$ in order to keep the temperature of the regulator inside its operational temperature range of −40 °C to +85 °C.

1.2 V PTH05050W The total input power for the 1.2 V voltage regulator is around 0.9 W. As the output current is below the efficiency peak of this regulator, the efficiency is only around 71 % and thus the power dissipated by the regulator is of the order of 270 mW. A thermal resistance of better than $130\,\mathrm{K\,W^{-1}}$ will keep the regulator inside the operational temperature.

IS61WV10248BLL-10TLI The power dissipation of the high-speed SRAM is taken from the datasheet, which gives a maximum of 220 mW at a supply voltage of 2.2 V and an operating frequency of 50 MHz. As the memory is operated at a higher voltage of 2.5 V but with a lower frequency of 40 MHz, it is assumed that this value is still valid for an estimation. As the SRAM is only active when an L1 trigger is received, and the power dissipation is only around 80 mW when not active, the mean power dissipation will be much lower. Therefore, the power dissipation of the SRAM is not regarded as critical, but its temperature was explicitly monitored during the thermal tests.

XCF32P-VOG48C Similar considerations apply also to the platform flash PROM. The power dissipation in active mode is of the order of 150 mW, but only 5 mW in standby mode. As the PROM is only active after power on for less then 100 ms, it is not considered critical.

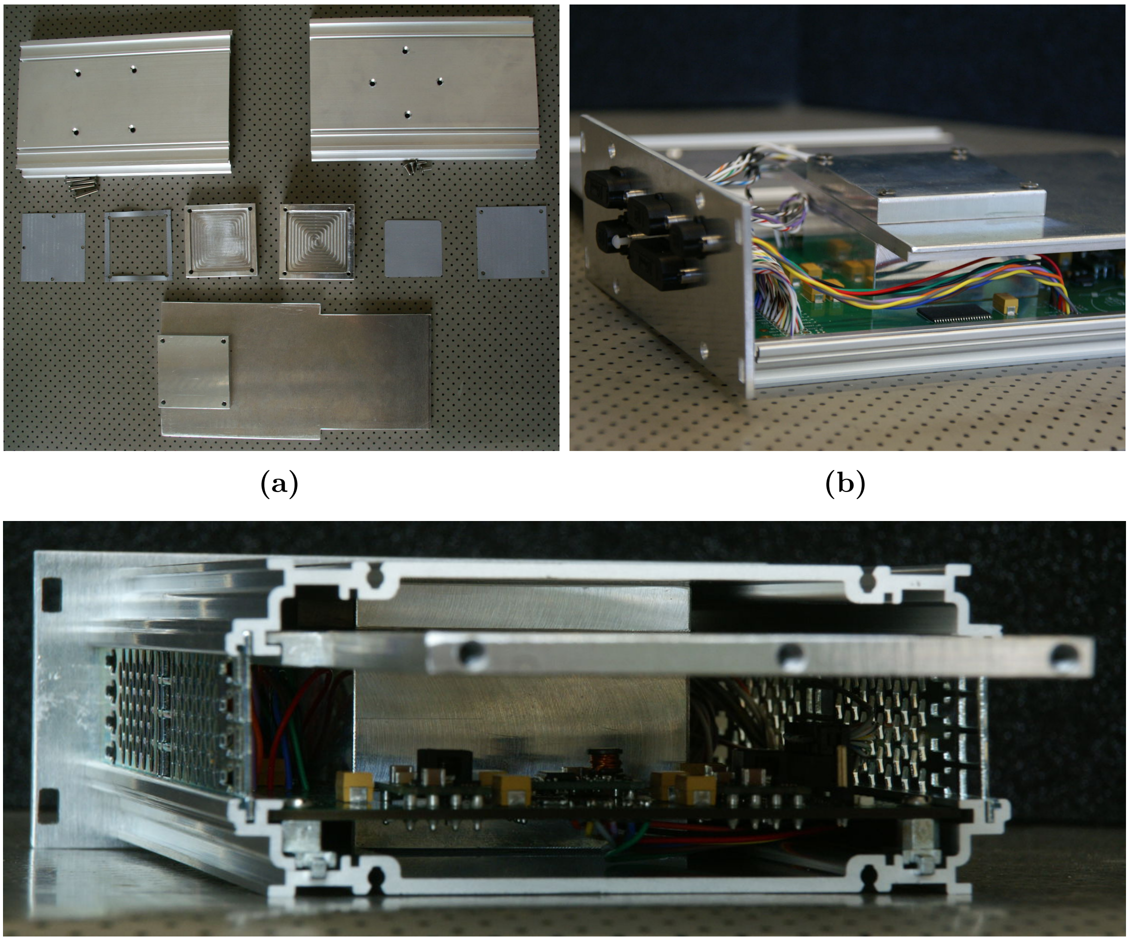
From this overview, it can be clearly seen that the most critical component which could reach a temperature outside its operational temperature range is the FPGA, and that only the hot case must be considered critical.

To reach a thermal resistance of only $R_\theta = 12.5\,\mathrm{K\,W^{-1}}$ between the junction of the FPGA and the radiator of the electronics – which is part of the mechanical support structure and connected to the main radiator at the top of the instrument – a dedicated heat sink was designed.

As mounting a heat sink onto the power supply modules was not feasible because of the very tight space available on the top side of the modules to reach the critical parts, and especially because the bottom side of the modules is not accessible at all, additional effort was put into the layout of the CCB in order to dissipate this power through the board itself. This is also important because part of the power of the FPGA is dissipated into the board. While the main power is dissipated through the heat spreader of its case due to the low thermal resistance of only $R_{\theta JC} = 0.2\,\mathrm{K\,W^{-1}}$ between the junction and the case, the thermal resistance between the junction and the board is of the order of $R_{\theta JB} = 2.5\,\mathrm{K\,W^{-1}}$ and thus cannot be neglected. In addition, a total of around 1 W, dissipated by the remaining components like the power supply modules, clock drivers, or ADC, has to be removed via the PCB.

To efficiently transfer the heat from the board, additional copper layers have been implemented together with a thermal contact area around the FPGA, onto which the heat sink is mounted – this is visible as a golden, rectangular structure in Figure 5.4. To electrically decouple the heat sink and to improve the thermal contact between the FPGA, the PCB, and the heat sink, an isolating but thermally conductive filler material is used which does not outgas in the low-pressure environment during the balloon flights. In particular, a fiberglass reinforced silicone rubber pad with a low thermal resistance was selected (Sil-Pad 400).

An additional constraint put on the overall mechanical design is directly deduced form [MRA4] (see Sections 3.2.1 and 3.3), and had to be taken into account while designing the heat sink. As the instrument has to withstand a shock of 10 g when the parachute opens, the mechanical fixation of the heat sink was considered as critical.



(a) (b)

(c)

Figure 5.5: Thermal structure of the CCB and its assembly. The different parts are shown in (a), which are from top to bottom: the two sides of the case, the two aluminium blocks which are mounted directly to the FPGA and the PCB (together with the thermal pads on the left and right), and the main aluminium plate which provides the thermal contact to the radiator (together with the small block which provides additional mechanical support). The partly assembled heat sink is shown in (b), and the final assembly in (c). To provide a better insight, the rear side of the case is not closed.

In order to avoid any damage to the board or the soldering of the FPGA, and at the same time provide a good thermal interface between the FPGA, the PCB, and the radiator, the heat sink is designed as follows (see also Figure 5.5):

- An aluminium block with a pocket on the bottom is placed on top of the FPGA and provides the main thermal interface for the FPGA and the board.
- A similar block is mounted on the bottom side of the CCB to provide an additional thermal interface for the board. Both blocks are fixed to the board itself with a defined pressure, in order to improve the thermal contact.
- The block on the bottom side of the board is mounted to the case of the CCB, which reduces the mechanical stress on the board.
- An aluminium plate is mounted to the upper block and provides the main thermal interface towards the radiator. This plate has a mechanical interface with the case and the radiator, in order to mechanically support the whole structure and keep the mechanical stress away from the board.
- To further support the heat sink, an additional block is mounted into the space between the plate and the other side of the case. This provides an additional mechanical interface between the heat sink and the case.

The whole thermal structure was successfully tested in a thermal vacuum chamber with the CCB as standalone module and validated in a large scale thermal vacuum test with the complete electronics of the instrument integrated (see Section 6.4.1).

5.2.3 L2 trigger

The central functionality of the CCB is the reduction of the fake trigger rate to a level compliant to the data downlink bandwidth of the experiment. Therefore, the 'Linear Track Trigger' module, which implements the L2 trigger algorithm with Very high-speed integrated circuit Hardware Description Language (VHDL) inside the FPGA, is the most important one, and also consumes most of the available resources of the FPGA. A block diagram of the internal logic of the FPGA – with focus on the L2 implementation – is given in Figure 5.6.

A first implementation of the L2 trigger algorithm (described in Section 2.4.2) was developed in Bayer, 2011. This implementation was further optimized and adapted to the final data interface between the CCB and the PDM and to the SRAM (see also Bayer et al., 2011, 2013). To fulfill the requirements on the processing time and to reduce the impact on the dead time of the instrument on the one hand, while remaining compliant with the area constraints of the FPGA on the other hand, a highly parallel and pipelined architecture was combined with fast serial processing.

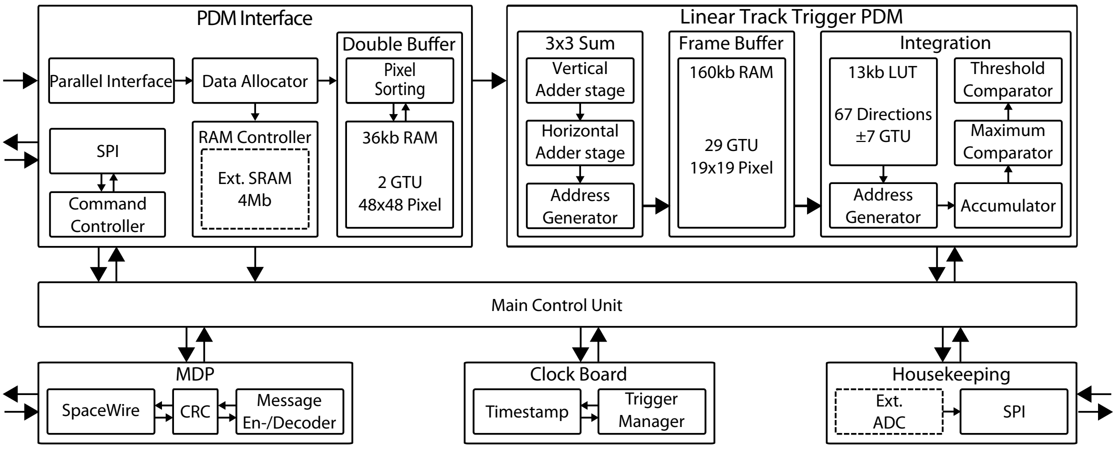


Figure 5.6: Block diagram of the logic implemented in the FPGA of the CCB for EUSO-Balloon and EUSO-SPB with focus on the implementation of the L2 trigger algorithm. (Image adapted from: Bayer et al., 2013)

It should be stressed that this module – together with the PDM interface and the SRAM controller – has to be implemented eight or nine times for the JEM-EUSO CCB.

Upon arrival of the scientific data from the PDM, the 'Data Allocator' routes the raw data stream to the 'RAM controller', which writes the data to the external SRAM. When the evaluation of the L2 trigger is finished, the data will be read back and sent to the MDP via the SpaceWire interface, or simply discarded if no L2 trigger is issued. At the same time, only the photon counting data per GTU are selected from the data stream and written to a 'Double Buffer' module, which is implemented inside the internal memory of the FPGA. Before the data are actually written into the double buffer, the pixels are sorted in a way to resemble a 48×48 pixels picture. As the L2 trigger algorithm is based on the geometrical and temporal properties of the shower, but the mapping between PDM pixel and ASIC channel is not straight forward[22], this sorting is done in order to simplify the subsequent processing. By implementing a double buffer structure, it is possible to receive, sort and write the next GTU frame, while the previous one is still processed.

From the 'Double Buffer', the data are transferred to the 'Linear Track Trigger' module, which performs in a first step ('3×3 Sum' module) the summation of the 3×3 pixels boxes. This summation is done inside two pipelined modules – one for the vertical and one for the horizontal sum – whereof each consists of a parallel 3-input adder stage. As only a specific part of the data around the trigger seed (which is the position of the L1 trigger) is needed for the final integration along the

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[22] This is because the ASIC-channel to MAPMT-anode mapping is driven by hardware and layout constraints.

predefined directions, the following ‘Address Generator’ writes only these data to an additional ‘Frame Buffer’. After all data are written to the buffer, it contains ± 14 GTUs and 19×19 ‘pixels’ around the trigger seed, whereof each ‘pixel’ is the sum of the surrounding pixels from the original frame – this way, no redundant 3×3 sums are being performed.[23] In the last ‘Integration’ module, an additional ‘Address Generator’ reads the different 3×3 sums from the ‘Frame Buffer’, which are necessary for the integration along a particular direction, and allocates these data to an accumulator which performs the final integration. The correct addresses inside the ‘Frame Buffer’ are calculated by the ‘Address Generator’ depending on the current starting point and the offsets for the current direction from this starting point. As these offsets are pre-calculated and stored in a Look Up Table (LUT), they can be adapted easily to a different configuration of the instrument (e.g., change in the optics or the height of the orbit). Because the 3×3 summation was already done in advance, the amount of read cycles from RAM necessary for the integration is greatly reduced – instead of reading 9 pixels per 3×3 sum, only one read access is necessary. In the end, the ‘Maximum Comparator’ selects the overall maximum of the integration, and a simple ‘Threshold Comparator’ issues the L2 trigger in case the maximum exceeds the set threshold.

This final integration is done serially, which reduces the amount of logic resources while keeping the overall processing time low. In fact, the total processing time is around 5.7 ms, and the evaluation of the trigger is actually finished before all data are received from the PDM – thus, the L2 trigger algorithm does not add any additional dead time to the instrument (see also Section 6.4.3).

5.3 EUSO-SPB Photo-Detector Module Control Board

The development of the PDM control board started at the Ewha Womans University in Seoul and the Sungkyunkwan University in Suwon, Republic of Korea and was continued at the University Paris Diderot, France by Jung, 2017. This PDM control board was used in the pathfinder projects EUSO-TA and EUSO-Balloon to successfully demonstrate the detection principle of JEM-EUSO. But due to the tight schedule, the amount of resources available in the FPGA, and thermal issues arising from a high power consumption (which increases as more resources of the FPGA are used), the L1 trigger was not implemented (Jung, 2017).

In preparation of the EUSO-SPB project, a list of possible improvements has been

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[23] If the pixels would be first selected according to the current direction integration and then summed up, a huge amount of summations will be redundant because the same 3×3 boxes are used for different integrations. An obvious example is the central box around the trigger seed which is included in all direction integrations with the same start point.

compiled, which were identified during the EUSO-Balloon flight and the instrument integration. To fulfill the requirement on the detection of UHECR induced air showers with EUSO-SPB (see Section 4.1), the highest priority was allocated to the implementation of the L1 trigger. In order to reach this milestone, extend the functionality, and to improve the reliability of the PDM control board, a redesign was necessary. This was done in the framework of this thesis. The following section describes the hardware implementation of the new PDM with focus on these changes.

5.3.1 Implementation

In order to stay compliant with the project schedule, it was necessary to re-use the layout of the EUSO-Balloon PDM control board where possible, which, at the same time, puts stringent constraints on the possible improvements.

To make sure that the L1 trigger algorithm can be implemented successfully, a parallel strategy was followed. On the one hand, the originally chosen FPGA was replaced by a slightly larger FPGA from the same family, which is available in a pin compatible package (XC6VLX365T-1FFG1156), and on the other hand, the VHDL implementation of the L1 trigger was optimized (see Section 6.5.4).

For the storage of the firmware bitstream of the FPGA, the EUSO-Balloon PDM control board had a flash memory implemented which is optimized especially for the Virtex-5 and Virtex-6 configuration interfaces (XCF128X). Unfortunately, this memory was discontinued, and no direct replacement was available. With an industry standard Not OR (NOR) flash memory from Micron, a new solution was found, which had only minor impact on the layout. This memory is available in a footprint compatible package and thus only a few signals had to be changed or rerouted. In addition, it uses the same configuration interface of the FPGA which was already thoroughly tested during the EUSO-Balloon campaign, which simplified the qualification process (see also Section 6.5.1).

In contrast to the Virtex-4 used for the CCB, the Virtex-6 includes an ADC (System Monitor) which is internally connected to the voltage rails of the FPGA and the temperature sensing diode. An additional, external ADC has been implemented on the PDM control board, in order to monitor the board temperature and the voltages provided to the ASICs. Due to problems in the layout of the original PDM control board, it was not possible to use the internal ADC to monitor the voltages and the core temperature of the FPGA, and due to grounding issues, the monitoring of two of the ASIC voltages was also not possible. These issues were successfully solved in the re-design and the engineering data could be provided to the HK system.

Additional minor issues which were identified and corrected in order to increase the reliability of the PDM control board were:

- The LVDS receiver and transmitter implemented for two HK interface signals

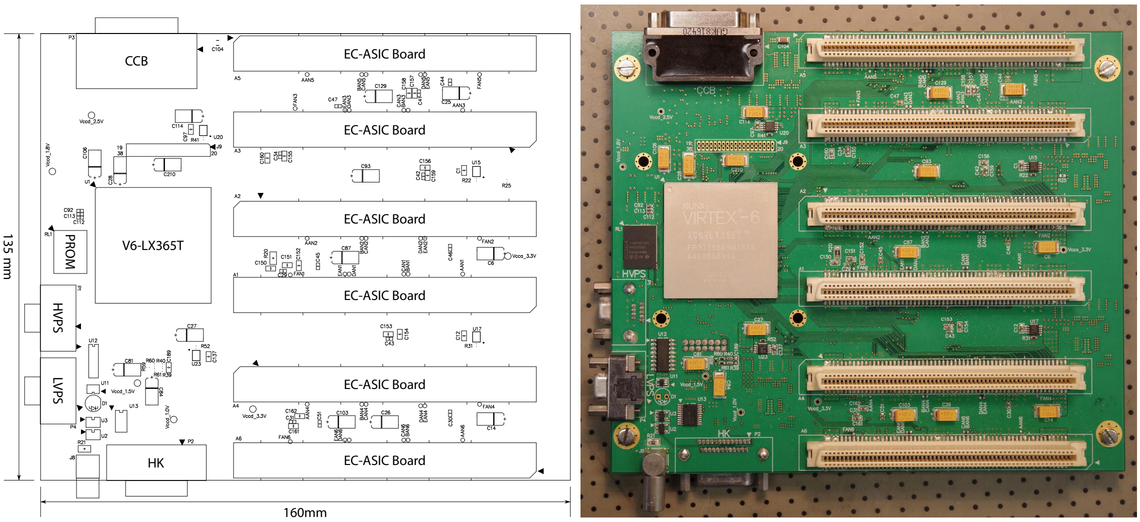

Figure 5.7: Schematic overview (left), and the assembled PCB (right) of the PDM control board which was developed for the EUSO-SPB project. The FPGA can be seen in the center of the left side of the board, while the largest part of the board area is devoted to the six connectors, which provide the interface to the SPACIROC 3 ASICs. The power supply is implemented on the rear side of the board.

were operated outside the recommended supply voltage and the termination resistor was missing. This issue was regarded as critical, because these signals are related to the configuration of the FPGA.

- The configuration interface of the FPGA can be changed by means of three signals which were connected to mechanical Dual In-line Package (DIP) switches. These switches are not very reliable and can fail or change state due to vibrations or shocks during the transportation to the launch pad or during the launch itself. If this happens, it is not possible anymore to load the firmware bitstream from the PROM and to configure the FPGA. In order to prevent this risk, the switches were replaced by soldered jumpers.

Besides the improvements on the level of the hardware, the firmware of the FPGA was completely re-written and highly optimized. This was mainly necessary because the amount of occupied logic resources had to be reduced, in order to implement the L1 trigger algorithm. In addition to the successful implementation of the L1 trigger, several issues were solved and new functionalities were implemented.

One of the central improvements of the EUSO-SPB detector was the replacement of the ASIC with its next generation, which offered a better performance and a lower power consumption. In order to support the new SPACIROC 3 ASIC, the module which handles the slow-control interface and the setting of the configuration parameters was re-written with a completely different architecture compared to the implementation for EUSO-Balloon. This new architecture not only greatly reduced the amount of resources needed, but also simplified the whole configuration process. In addition, the reliability of the interface was improved by the possibility to read-back the parameters from the ASICs, which is used to check if a transmission error occurred.

In order to protect the MAPMTs in case of bright light, the HVPS provides a general over-current protection which shuts down the HV. As this over-current protection is based on the overall current provided to the whole PDM, a localized bright light – as it can occur during a thunderstorm – could still damage or degrade a single MAPMT. Therefore, the HVPS provides an interface to the PDM control board through which the voltage of the photocathode can be changed. By increasing this voltage, the gain of the MAPMT is effectively reduced, which protects the MAPMT as the anode current is reduced. To make use of this interface, an algorithm was implemented inside the FPGA which monitors the amount of light reaching a single pixel (anode). As soon as the light exceeds a threshold, the gain is automatically reduced, and increased again, as soon as the light is back to a safe level (with some hysteresis). As the HVPS can change the voltage on the level of an EC, the remaining ECs are operating normally in case the algorithm triggers on a localized light source.

While not required for EUSO-Balloon, the fast automatic protection of the MAPMTs was important for the long duration EUSO-SPB flight. The results of the performance of the implemented algorithm are given in Section 6.5.5.

5.3.2 Power Supply & Grounding

The improvement with the biggest impact on the layout was related to the re-design of the power supply and the power distribution system. This was necessary and mainly driven by thermal and grounding issues of the EUSO-Balloon PDM module in addition to higher power requirements of the ASICs.

The grounding scheme of the original design was based on galvanically isolated Direct Current to Direct Current (DC/DC) converters and a strict separation of the various power rails and their grounds, like the analog and digital voltages for the ASICs or the FPGA (see also Jung, 2017). In preparation of the PDM control board re-design, the electrical architecture of the EUSO-Balloon instrument – especially the part related to the PDM control board – was analyzed, and an overview of the re-designed architecture is given in Figure 5.8. This architecture resembles the final implementation of EUSO-Balloon and includes various jumpers, which were soldered at several places in order to electrically connect the different grounds. These jumpers were added during the integration in order to mitigate issues with electrical noise and the interfaces which were not galvanically isolated. As it can be seen, all three isolated grounds between the PDM control board and the ASIC board are connected together. GNDA and GNDD are interconnected at the level of the ASIC boards via

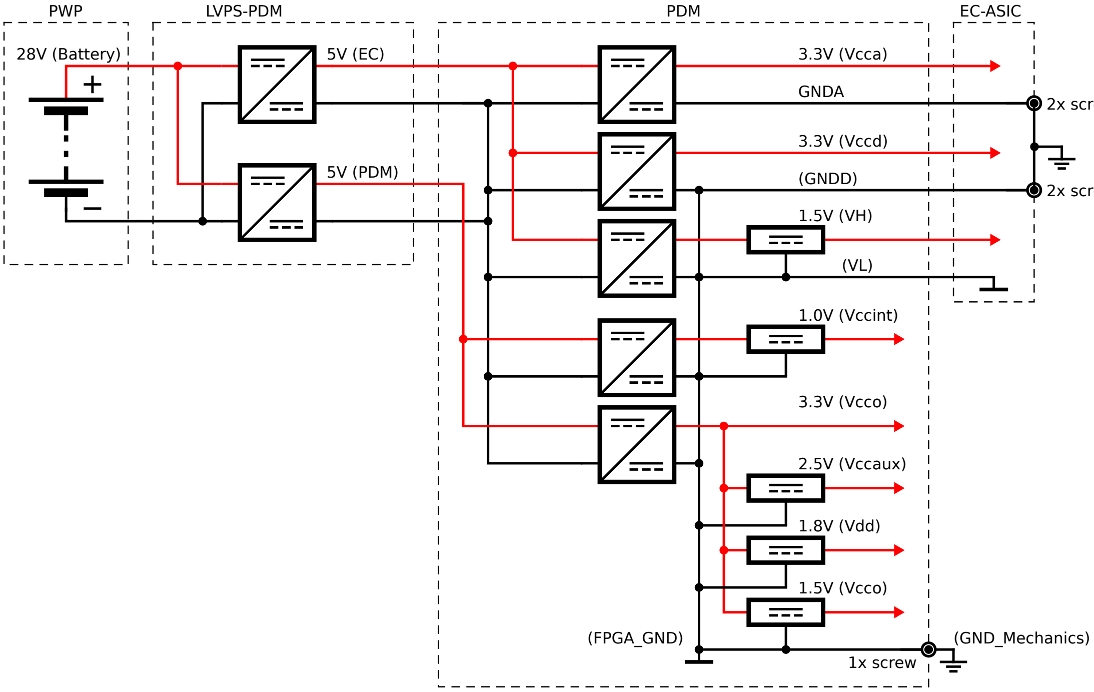

Figure 5.8: Part of the final electrical architecture related to the PDM control board as implemented in the EUSO-Balloon instrument.

small jumpers (which establish an electric connection between the grounds and two mounting holes each) and the mechanics or dedicated wires (which provides the electric connection between the mounting holes). At the level of the PDM control board, a connection between the FPGA ground (FPGA_GND) and VL is made via two soldered jumpers in addition to a connection between FPGA_GND and GNDD. Finally, the isolated grounds coming from the LVPS are also connected together at the level of the PDM control board.

By looking at the interfaces in detail, the associated issues are obvious. Vcca/GNDA is connected to the analog parts of the ASIC, but also includes the slow-control Flip-Flops (FFs). Therefore, it is mandatory to have a proper connection between GNDA and FPGA_GND to have a reliably slow-control interface to configure the ASICs. In the EUSO-Balloon implementation, the return currents for this interface have to flow through a jumper on the ASIC board to the screw-holes, through the mechanics (aluminium) to the second screw, through another jumper to the GNDD plane, and finally through a third jumper on the PDM control board to the FPGA_GND. Similar considerations apply to the fast data interface between the FPGA and the ASICs with VL as the reference potential. In the EUSO-Balloon implementation, the connection between VL and FPGA_GND is done with a single jumper on the PDM control board. This connection is shared by the return currents of 360 I/Os, and

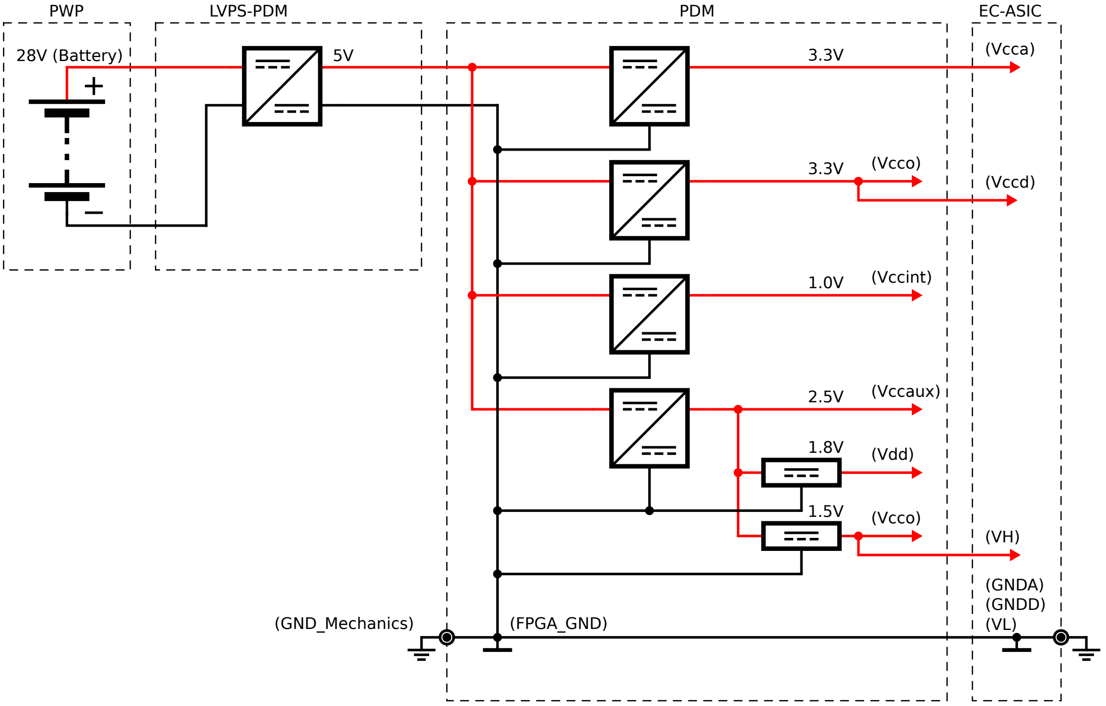

Figure 5.9: The power supply architecture of the EUSO-SPB PDM control board. The isolated DC/DC converters are replaced by non-isolated DC/DC converters. Therefore, especially the linear regulators are removed, which have a high power output and bad efficiency (e.g., for Vccint). At the same time, any switching noise generated by the FPGA or the digital part of the ASICs is kept away from the analog portion of the ASICs due to the physical separation by design.

because of the routing through a jumper the impedance of this return path is far from optimum. Finally, GNDD is the common mode reference for several LVDS signals between the PDM control board and the ASICs, and therefore has to be connected to FPGA_GND. Due to the differential architecture of the signals, the requirements are less demanding, as only a small common mode current will flow through this connection. Nevertheless, the requirement is that the common mode voltage has to be within $\pm 1\,\mathrm{V}$, which also applies to other interfaces like the ones towards the CCB.

As already mentioned, the main driver to change the design of the PDM control board power supply is the low efficiency and the resulting problems in removing the heat from the regulators. This applies especially to the linear regulator for the FPGA core voltage (Vccint), which has to deliver high currents but has a low efficiency of around 30 %. If the efficiency of the two DC/DC converters is included, the total efficiency goes down to around 20 %. The other implemented improvement deals with the grounding philosophy of the ASICs and the separation of the analog and digital grounds. Based on the EUSO-Balloon design, there is already a physical separation between the analog parts (analog section of the ASIC) and the digital parts (mainly the FPGA, but also the digital parts of the ASIC). Due to this physical separation by design, there is no need to deal with separate ground planes in order to keep the digital currents away from the sensitive analog parts. In addition, the EUSO-Balloon architecture did not fulfill the requirement to have a single short ground connection point (‘star’ topology/connection) of the analog/digital planes close to the ASIC[24], especially because there are 36 ASICs separated on 6 boards. Therefore, the suggestion given to the collaboration was to have a single ground on the PDM control board and the ASICs boards[25]. This new architecture, which is given in Figure 5.9, was finally accepted and implemented.

The 3.3 V analog voltage for the ASICs (Vcca) is provided by a dedicated non-isolated DC/DC regulator (LMZ31704), which is able to deliver 4 A with a peak efficiency above 95 % between 1 A and 3 A. As there was no requirement given on the maximum acceptable output voltage ripple, the specification from the old DC/DC converter was taken as a reference, which is given as 40 mV. The output voltage ripple of the new regulator is given by approximately 8 mV, thus exceeding the reference.

The 3.3 V digital voltage for the ASICs (Vccd) is now also used to supply the slow-control FFs inside the ASICs and thus for the slow-control interface and the level-translators on the PDM control board. This helped to solve the problems with the slow-control interface present in the EUSO-Balloon project. The power for this voltage rail is provided by an additional LMZ31704 regulator.

The 1.0 V core voltage of the FPGA (Vccint) is also generated by a dedicated non-isolated DC/DC regulator (LMZ31710) which is capable of delivering a maximum of 10 A, whereas the maximum efficiency is around 90 % between 2 A and 3 A. As the power consumption of the XC6VLX365T was estimated to be around 5 A to 6 A, this regulator includes enough margin.

The 2.5 V auxiliary voltage for the FPGA (Vccaux), which is also used for various other elements like the I/O drivers, the ADC of the system monitor, and the LVDS drivers/receivers, is again generated by a dedicated regulator (LMZ31704). The 1.5 V I/O voltage for the data interface towards the ASICs (VH) is generated from the 2.5 V rail with a simple linear regulator, because the power requirement is not too demanding and the efficiency of 60 % is in this case still acceptable. The same applies to the 1.8 V needed by the configuration PROM, which is only active while the firmware bitstream is loaded to the FPGA. This is a similar architecture as

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[24] A short connection is important in this design philosophy, as any additional inductance between the analog and digital reference will increase the noise coupled onto the analog side through stray capacitances inside the ASIC.

[25] A new layout for the ASIC boards was necessary anyhow in order to implement a new version of the ASIC – the SPACIROC 3.

it was implemented in the EUSO-Balloon PDM control board. Nevertheless, smaller regulators are used (TPS7A7001) which are supplied by the 2.5 V voltage rail instead of 3.3 V, in order to increase the efficiency.

In order to limit the inrush currents when powering the PDM control board, which led to problems in EUSO-Balloon, a power-on sequence together with soft-start circuitry was added. As no requirement is given for the power-on sequence of the ASICs, the two voltages are tracked and ramped up together. Therefore, the final implemented power-on sequence is:

- 1.0 V core voltage of the FPGA (Vccint),
- 2.5 V auxiliary voltage for the FPGA (Vccaux) together with 1.5 V and 1.8 V,
- 3.3 V analog and digital voltage for the ASICs (Vcca and Vccd) together.

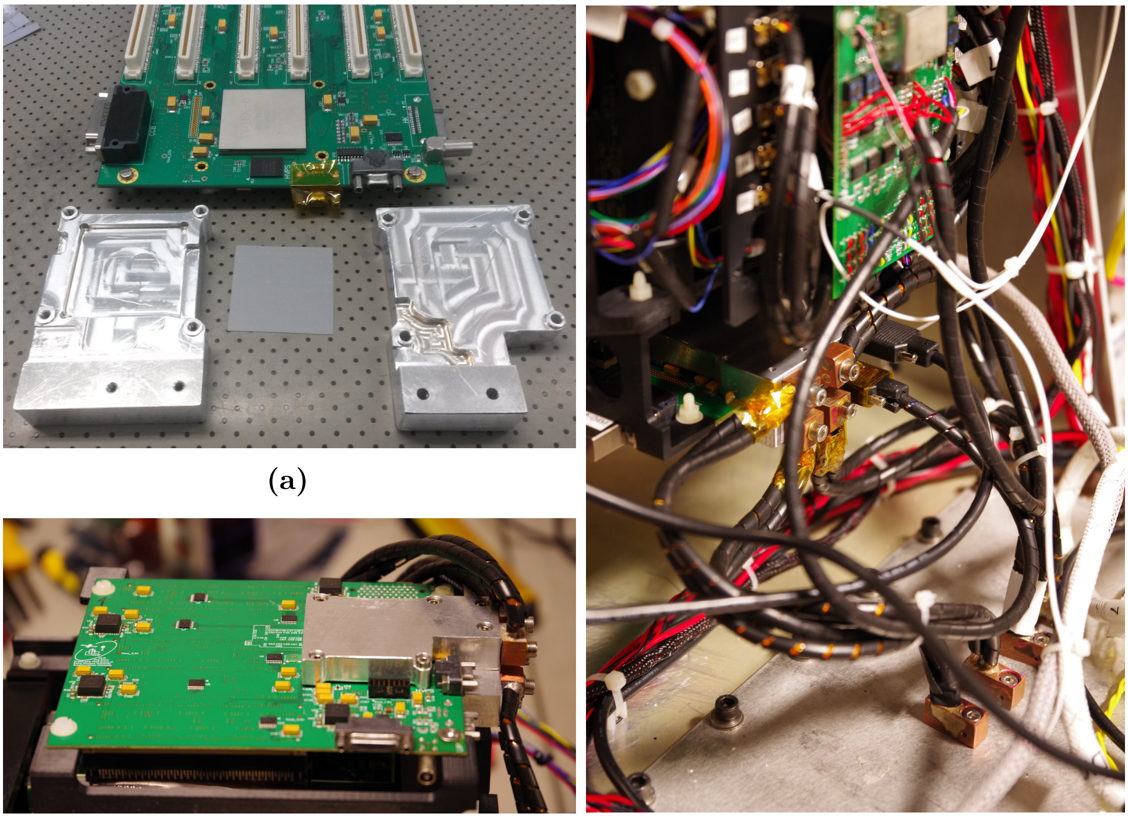
In addition, shunt resistors together with amplifiers are implemented in order to monitor the currents of the main voltage rails, which was not available in the EUSO-Balloon PDM control board.

This new architecture led to a general improvement of the electromagnetic compatibility. Together with a better high-frequency decoupling of the supply voltages because of an increased inter plane capacitance of the power supply distribution network, the overall electrical noise coupling into the ASICs was reduced. Thus, an increase of the signal to noise ratio of the instrument was obtained.

5.3.3 Thermal structure

During the first thermal tests, the EUSO-Balloon PDM control board had thermal issues, resulting in a shut-down of the FPGA – this issue had to be solved for the EUSO-SPB PDM control board. In particular, the FPGA and the linear voltage regulator for the FPGA core voltage were identified as critical components with the highest power dissipation. As the layout did not account for a thermal structure, a large aluminium plate was mounted on the back side of the board. The thermal contact was then established with copper braids, which were glued to the critical parts. As the total thermal resistance for this interface was too high, the internal thermal protection of the regulator was activated when the internal temperature reached 165 °C. This happened during the thermal tests when reaching the hot case of the test cycle (see 6.4.1). This thermal protection disables the output of the regulator in order to avoid damaging the regulator, which effectively switches off the FPGA.

Based on the experience with the thermal structure of the CCB (see Section 5.2.2), a similar heat sink for the FPGA and the board was designed (see Figure 5.10). As the complete PDM is mounted on a translation stage in order to adjust to the two different focal points for the two- and three-lens design, the thermal interface



(a)

(b)

(c)

Figure 5.10: The thermal structure of the EUSO-SPB PDM control board consists of two parts (a). One half is mounted on the top side of the board and mainly interfaces with the FPGA, which dissipates most of the power, while the other half is mounted on the bottom side (b) to remove the power dissipated into the board mainly by the voltage regulators and the FPGA. The thermal interface between the heat sink itself and the radiator of the instrument is established with flexible copper braids, in order to fulfill the requirement of an adjustable focus of the PDM. A total of eight copper braids are used, which can be seen in (b) on the right side of the heat sink, and in (c) as black wires due to their insulation in order to avoid any short circuit in case they touch the electronics. They are running from the heat sink, which is visible in the center of (c), to the radiator (bottom right corner).

between the heat sink and the radiator is established via thick copper wires and thus is flexible. Due to the re-design of the power supply, a dedicated heat sink for the linear regulator was not needed anymore, because the efficiency was increased from around 30 % to about 90 %. The remaining power is dissipated into the board and removed from there by the heat sink and the radiator.

6 Performance and Results

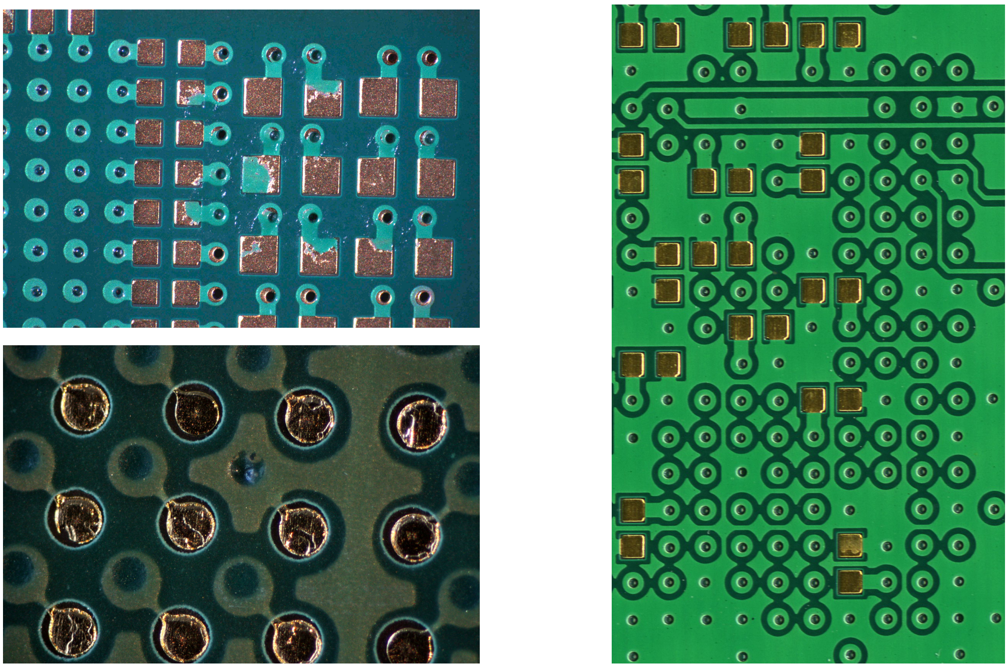
The performance and the functionality of the hardware, which was developed within the framework of this thesis, was tested and verified during several test campaigns at different assembly levels (from single components up to field tests of the fully integrated instrument) and finally during the EUSO-Balloon and EUSO-SPB balloon flights.

The following chapter presents these results, which includes aspects of the hardware manufacturing, of the soft- and firmware development and the in-flight performance.

6.1 Manufacturing

The production of the board and the soldering of the parts was done in collaboration with industry partners. Although the manufacturing of the board did not require any new technology, it was still challenging due to its 16 copper layers (8 for the EUSO-Balloon and EUSO-SPB CCB), design structures of 100 µm, and the need for controlled impedance (see Section 5.1.3). In addition, the escape vias under the BGA of the FPGA were filled or 'plugged' and covered with a solder mask. The covering was done to avoid possible problems related to the soldering of the FPGA where the solder ball could flow into the escape via instead of creating a reliable solder joint. The plugging of the vias was required to avoid the possible trapping of chemicals from the manufacturing process (or air) inside the via, which could create problems when operating the board in vacuum or in a low-pressure environment as it is the case for EUSO-Balloon and EUSO-SPB. The technological challenges associated with the production of the boards becomes clearer when looking at the manufacturing failures encountered: the JEM-EUSO and the EUSO-Balloon prototype CCBs had issues with the plating of the pads such that the parts could not be soldered reliably (see Figure 6.1a), the EUSO-Balloon flight model had issues with the size of the structures such that the ground and power planes were not continuous anymore and contained copper islands (see Figure 6.1b), which affects the trace impedance and the decoupling network, thus increasing the general electrical noise. Only the EUSO-SPB flight model PCB batch was manufactured without flaws and did not have to be rejected and re-produced.

The soldering of the BGA of the FPGA was regarded as a critical process due to its large size and the involved risk of not evenly heating up the whole package, which could result in bad solder joints or overheated components. Therefore, the



(a) **(b)**

Figure 6.1: Manufacturing issues of the different CCB versions. (a) shows issues in the gold plating of the solder pads which was partially missing or not perfectly even. Issues with the size of the design structures are shown in (b). This lead to copper islands especially inside the escape via array of the FPGA resulting in split power- and ground planes.

component mounting was done with vapor-phase soldering, which is also commonly used to manufacture space-grade electronics as it allows an exactly defined maximum temperature (defined by the boiling point of the liquid used) and an efficient heat transfer. To verify the soldering quality of the BGA and the Quad-Flat No-leads (QFN) packages, X-ray images were taken from the assembled boards (see Figure 6.2). The images reveal possible defects or displacements, and the amount and size of voids (i.e., trapped gas) inside the solder balls can be measured. Voids can impact the signal integrity, power dissipation, and the reliability of the solder joint, and are a major issue especially in lead-free soldering. While some studies show that a certain degree of voids can even increase[1] the reliability of the solder joint (Hillman et al., 2011), large voids are generally considered to compromise the strength of the solder joint as they can be a source for micro cracks – this is especially important when

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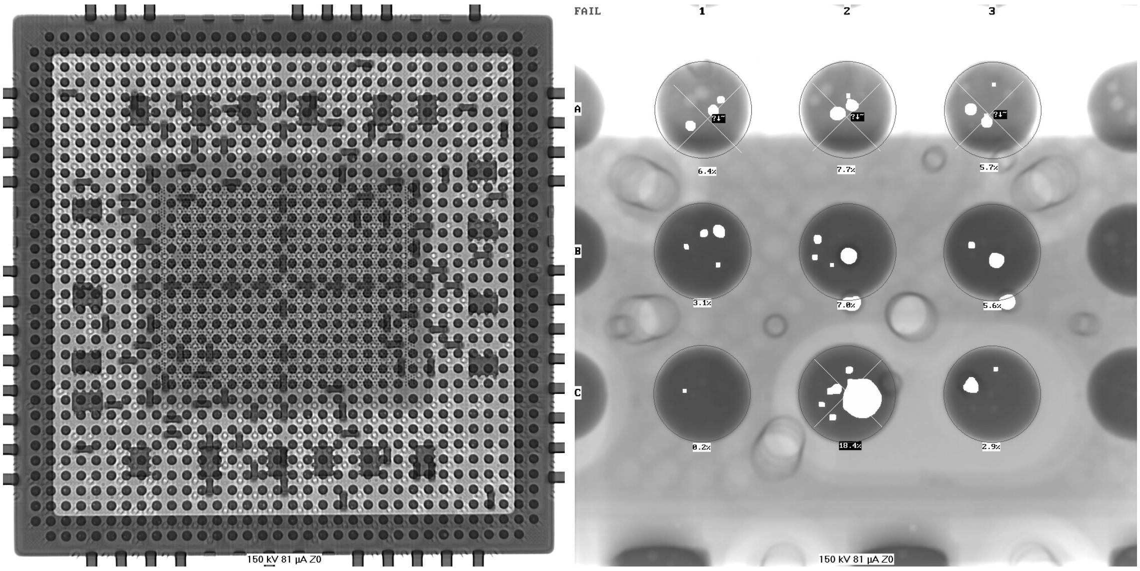
[1] Small voids can create a more flexible ‘spongy’ solder joint and can help stopping the further propagation of a micro-crack once it is formed.



(a) **(b)**

Figure 6.2: X-Ray picture of the FPGA mounted on the EUSO-Balloon CCB flight model. (a): The solder balls from the BGA are visible as filled, dark-gray circles and the voids as small light-gray areas inside the balls which are marked in white on the magnification, shown in (b). The biggest void found was measured to be 18.4 % of the (projected) area from the ball, which was acceptable especially as the vast majority of the voids were of the order of a few percent. The escape-vias of the PCB are visible as non-filled light-gray circles between the balls, and a close look also reveals the micro-solder balls (or ‘bumps’) on the silicon die (large light-gray filled rectangle in the center) from the Flip-Chip package. The dark-gray rectangles are decoupling capacitors placed inside the FPGA package (large rectangles surrounding the die) or on the bottom side of the PCB (small rectangles). The outline of the package can be seen as a dark-gray rectangular frame which is visible due to the copper heat-spreader of the package (see also Xilinx, 2006).

operating in vacuum or low-pressure environments and for components subject to high thermal stress. The largest void found on the EUSO-Balloon CCBs was 18.4 % of the area, which was acceptable and there was no need to adjust the process parameters, especially as other voids were only of the order of a few percent.

The measurement of the impedance for the different single-ended and differential structures was done by the company who manufactured the PCB. As it can be seen from the measurement protocol given in Table 6.1, the calculated widths of 100 µm for the single-ended traces on the top and bottom layer were slightly outside the given tolerance of ±10 %, but was regarded as acceptable and no changes were required. For the differential traces on the internal layers (designed as offset striplines), the

Table 6.1: Impedance measurements for different trace geometries and signal layers of the CCB. The target impedance of $(50 \pm 5)\,\Omega$ for single-ended traces on the top and the bottom layer was reached for 125 µm wide traces and slightly missed for 100 µm wide traces. The differential target impedance of $(100 \pm 10)\,\Omega$ was reached on the inner layers by reducing the trace distance to 150 µm and on the outer layer by slightly adjusting the geometry. Both changes were done by the manufacturer by means of a thinner pre-preg (150 µm instead of 200 µm) and by adjusting the traces (from 100/150 µm to 114/135 µm).

Single-Ended Layer	Trace width	Target	Measurement
L1	100 µm	50 Ω	56.50 Ω
L16	100 µm	50 Ω	55.80 Ω
L1	125 µm	50 Ω	50.69 Ω
L16	125 µm	50 Ω	50.71 Ω

Differential Layer	Trace width/distance	Target	Measurement
L1	114/135 µm	100 Ω	102.3 Ω
L16	114/135 µm	100 Ω	97.8 Ω
L3	100/150 µm	100 Ω	98.5 Ω

distance was slightly adjusted from 200 µm to 150 µm by using a thinner pre-preg[2] (see also the layer stack of the CCB in Section 5.1.3), while the trace geometry (width/distance) of the differential pairs on the top and the bottom layer was slightly adjusted from 100/150 µm to 114/135 µm.

6.2 FPGA Configuration

The FPGA needs to be configured each time it is powered up or after a power cycle has been performed. This is because the internal configuration memory is based on volatile SRAM cells and therefore, the bitstream – the application-specific configuration data or firmware – has to be loaded from an external non-volatile memory. For this purpose, the Virtex-4 provides different configuration modes, which

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[2] Pre-preg is an abbreviation for 'pre-impregnated'. In multilayer PCB manufacturing, glass fibers, which are pre-impregnated with uncured resin, are used as bonding sheets between the etched copper foils or the etched cores. A core is a pre-manufactured and cured pre-preg which has the copper foils already laminated.

differ in the role of the FPGA (master or slave) and in the width of the data interface (serial or parallel). While the 'slave' mode is typically used to configure a second daisy-chained FPGA or to load the bitstream with an external MCU, the width of the data interface basically defines the time needed to load the bitstream (together with the clock frequency). Even though the overall start-up time of the FPGA is not regarded as critical for JEM-EUSO[3], the CCB provides the possibility to evaluate the different modes. In particular, the master parallel mode (called 'Master SelectMAP' by Xilinx) is regarded as baseline mode as it provides the fastest configuration interface. At the same time, it requires the most I/Os and the data bus even shares GPIOs of the FPGA, which has to be taken into account especially because the CCB requires a lot of I/Os to implement the various interfaces.[4] As an advanced option, the possibility to change the configuration of the CCB during its operation in orbit was under discussion. This could be provided by configuring the FPGA with the MDP through the slave mode configuration interfaces.

In 'Master SelectMAP' mode, the clock for the configuration interface is generated by an internal Resistor-Capacitor (RC)-oscillator whose frequency can be programmed between 4 MHz to 60 MHz in several steps. Due to the temperature dependance of the RC network and manufacturing variability, the generated frequency is subject to a rather large variance of ±50 %, which has to be taken into account in order to stay within the timing requirements of the PROM. The minimum possible clock period T_{CYC} of the XCFxxP PROMs for the 'Master SelectMAP' mode with an I/O supply voltage of $V_{CCO} = 3.3\,\mathrm{V}$ is (Xilinx, 2010a)

$$T_{CYC,min} = 30\,\mathrm{ns}.$$

In addition, also the timing requirements of the FPGA have to be taken into account. In order to avoid any violation of the data setup timing, the minimum setup time $T_{SMDCC,min}$ (Xilinx, 2008b) for the data inputs of the FPGA has to be considered and added to the clock-to-data delay $T_{CAC,max}$ of the PROM:

$$T_{CYC} = T_{CAC,max} + T_{SMDCC,min} = 25\,\mathrm{ns} + 2\,\mathrm{ns} = 27\,\mathrm{ns},$$

and therefore, the $T_{CYC,min}$ does not violate the FPGA timing. Including the 50 % variance (worst case) of the RC-oscillator, the minimum period is

$$T_{CYC,config} = 41\,\mathrm{ns} \quad \text{or } f_{config} = 25\,\mathrm{MHz},$$

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[3] It is not foreseen to frequently power-cycle the instrument.

[4] In the prototype implementation of the CCB, the configuration data bus is shared with the data bus of the additional flash memory (see Section 5.1.2.1).

and the internal oscillator should be programmed to $f_{RC} = 20\,\mathrm{MHz}$, which is the next available setting and should be safe to use over the specified temperature- and voltage-range.

Measuring the resulting frequency for a given setting at room temperature shows that the RC-oscillator of the mounted FPGA is on the slower end of the variance, and the maximum setting of 60 MHz results in generated 39.37 MHz or $T_{CYC,config} = 25.4\,\mathrm{ns}$, which does not change within the ±5 % range of the operating supply voltage. Despite the fact that this $T_{CYC,config}$ is faster than the specified $T_{CYC,min}$ of the PROM, the bitstream is correctly loaded, which is validated with a Cyclic Redundancy Check (CRC) at the end of the configuration process. At this frequency, the whole configuration process takes just 153 ms compared to 484 ms at the 'safe' setting, which results (for the CCB FPGA) in an $f_{config} = 12.35\,\mathrm{MHz}$. It is easily estimated that the master serial mode will take eight times longer compared to the parallel mode as the data bus is eight bits wide. Therefore, the configuration time for the 'safe' setting will be around 4800 ms.[5]

As the configuration memory of the FPGA used for EUSO-Balloon and EUSO-SPB is smaller, only one PROM is used but the interface stays the same. Measuring the frequency of the internal RC-oscillator for the flight and spare models shows basically no difference between the different FPGAs and is similar to the one from the CCB FPGA. Programming the oscillator to its 60 MHz setting, results in a generated frequency of around 40 MHz and therefore, the total configuration time for these boards is only around 100 ms for the highest frequency setting. Again, as the configuration time and therefore the start-up time of the CCB is not regarded as a critical parameter, there is no need to operate the configuration interface at the limit of its specification or even above. The proper configuration over temperature and voltage range was thoroughly validated for the EUSO-Balloon and EUSO-SPB CCBs during development, testing, integration, and especially during the thermal vacuum tests (see Section 6.4.1). A frequency of 40 MHz for the configuration interface was kept during the flights.

6.3 JEM-EUSO Cluster Control Board

6.3.1 Ethernet Performance

To test the implementation of the Ethernet PHY and its Gigabit Media Independent Interface (GMII) with the FPGA, a test setup was prepared which is based on Xilinx, 2010e and uses the embedded Tri-Mode Ethernet Media Access Controller (EMAC)

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[5] As the timings for the serial mode can be slightly faster compared to the parallel mode, the f_{config} could be set to 26 MHz, which leads to a configuration time of the order of 3000 ms.

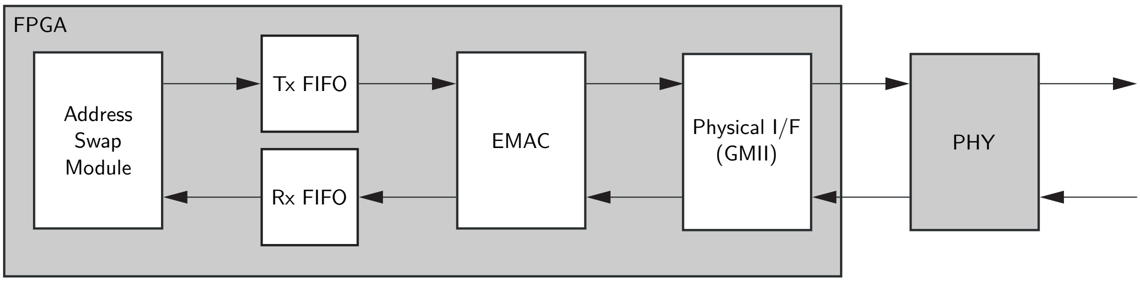

Figure 6.3: Basic setup used to test the proper implementation of Ethernet PHY which is connected to the FPGA via the GMII. Inside the FPGA, the GMII signals are routed to the EMAC which writes the received packets into a FIFO. From there, they are read by the 'Address Swap Module', which simply exchanges the source address with the destination address of the Ethernet frame and writes it back to the transmit FIFO. Therefore, any Ethernet packet received by the CCB will be sent back to its origin where it can be checked for transmission errors.

of the Virtex-4. As depicted in the block diagram given in Figure 6.3, the EMAC is connected to a receive and a transmit First In First Out (FIFO) buffer, which holds the received Ethernet frame, or the ones to be transmitted. The EMAC also provides the necessary signals for the GMII, which are routed to the I/O buffers of the FPGA and finally to the PHY via the PCB.

As soon as an Ethernet frame is received by the EMAC, an additional module reads it from the receive FIFO, swaps the source address with the destination address, and writes it back into the transmit FIFO. From there, it will be transmitted by the EMAC to the PHY and back to its origin. Thus, connecting the CCB with an Ethernet cable to a computer allows to send Ethernet packets to the board and to inspect the received packets for any transmission error.

The setup was successfully tested with an Ethernet data rate of 1000 Mbit s^{-1} (1000BASE-T, full duplex), for which the 8 bit parallel data interfaces (transmit and receive) between the FPGA and the PHY (the GMII) were running at 125 MHz. Other modes supported by the PHY (100 Mbit s^{-1} and 10 Mbit s^{-1}) and the auto-negotiation between connected devices were also tested successfully.

6.3.2 PowerPC 405

As an advanced option for the JEM-EUSO CCB, it is considered to use the embedded PPC405 cores for high-level data and command processing. To get a first idea on its performance, a system was set up to measure the data throughput of generated and processed Ethernet frames. The very basic components implemented are shown in Figure 6.4 and include

- a 256 Kibit large Block Random-Access Memory (BRAM) for the code and data processing,

- an INTerrupt Controller (INTC) used to signal to the CPU that an Ethernet packet has been received,
- some GPIO connected to LEDs for basic status information,
- an UART to interact with the running program, and
- the EMAC for the Ethernet connection which in turn is connected to the Ethernet PHY via the GMII.

The components are interconnected via a 32 bit wide Processor Local Bus (PLB) running at 100 MHz, while the PPC405 core is running at 200 MHz.

The software running on the PPC405 is based on Xilinx, 2012 and implements the LightWeight Internet Protocol (lwIP) stack, which is an open source TCP/IP stack developed with focus on low resource usage, which makes it suitable for embedded systems with only a small amount of available RAM and Read-Only Memory (ROM). On top of that, an implementation of a software called iperf[6] is running. Iperf is an open source software which is widely used to measure the network performance between two nodes and implements a server/client architecture which exchanges data to measure the throughput.

Connecting the CCB to a desktop computer and running the software shows that already this simple setup can achieve a data throughput of around 60 $\mathrm{Mbit\,s^{-1}}$ when the PPC405 acts as server (data sink), and around 55 $\mathrm{Mbit\,s^{-1}}$ when configured as client (data source). It should be stressed that this setup can be greatly enhanced by implementing for example higher clock frequencies (the PPC405 together with the PLB can run at up to 350 MHz for the slowest speed grade), faster RAM with Direct Memory Access (DMA) for the EMAC, or implementing larger data and instruction caches (see also Section 6.3.3).

6.3.3 DDR-SDRAM

To study the advanced option of using one large memory for the storage of the scientific data during the processing of the trigger instead of individual small memories, a 1 Gibit large DDR-SDRAM is implemented on the CCB (see also Section 5.1.2.1). To validate its implementation and the critical routing of the signals (see Section 5.1.3) between the FPGA and the memory chips, a more advanced embedded system was set up, which is based on Xilinx, 2008a and shown in Figure 6.5. The memory controller handles the interface to the external DDR-SDRAM and provides four dedicated ports:

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[6] Iperf stands for Internet Performance Working Group.

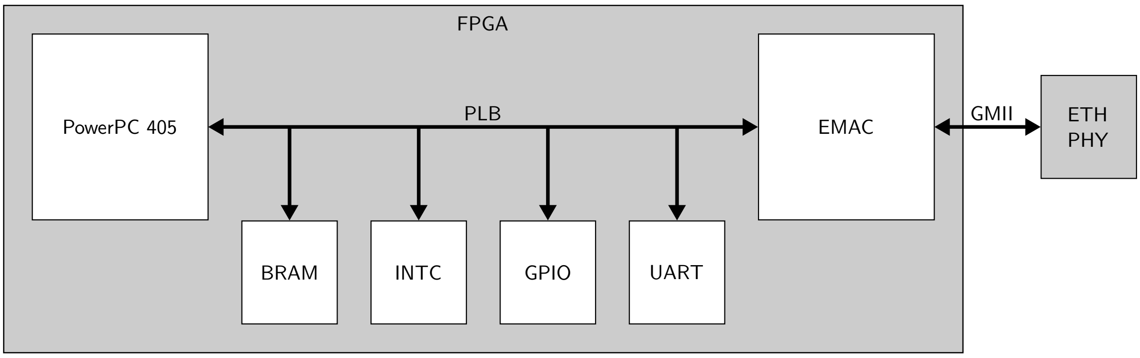

Figure 6.4: Block diagram of a first data throughput test setup based on the PPC405 core available in the Virtex-4 FX family. The main component on the PLB is the EMAC for the implementation of the Ethernet interface, which in turn is connected to the Ethernet PHY via the GMII. Additional periphery includes internal BRAM for the code and data processing, an INTC which issues an interrupt request to the CPU in case an Ethernet frame is received, and GPIOs connected to LEDs together with an UART module for monitoring and control purpose.

- two are used by the processor for data and instructions,
- one for the EMAC to implement the DMA,
- and one connected directly to the PLB.

Similar to the setup described in Section 6.3.2, the PPC405 core clock was set to 200 MHz and the PLB clock to 100 MHz. The DDR-SDRAM clock was set to 100 MHz[7], which leads to a memory bandwidth of 6.4 Gbit s^{-1} due to the Double Data Rate (DDR) and the 32 bit wide data interface. It should be stressed that this data rate is a theoretical value and the achievable data throughput is lower due to the necessary refresh cycles and the latencies or access times associated with Synchronous Dynamic Random-Access Memorys (SDRAMs).

A first memory test which writes various data patterns to all addresses of the DDR-SDRAM did not show any errors in the implementation of the memory at 100 MHz and was passed successfully. An additional implementation of the same iperf software as used for the PPC405 performance test (see Section 6.3.2) allowed to compare the two systems and showed an increase in the data throughput to around 80 Mbit s^{-1}. It should be pointed out that DMA was not yet used in this test but due to the DDR, the theoretical bandwidth was twice as large as compared to the implementation with the internal BRAM, that was also running at 100 MHz with a 32 bit wide data interface.

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[7] The implemented memory supports a maximum clock rate of 200 MHz.

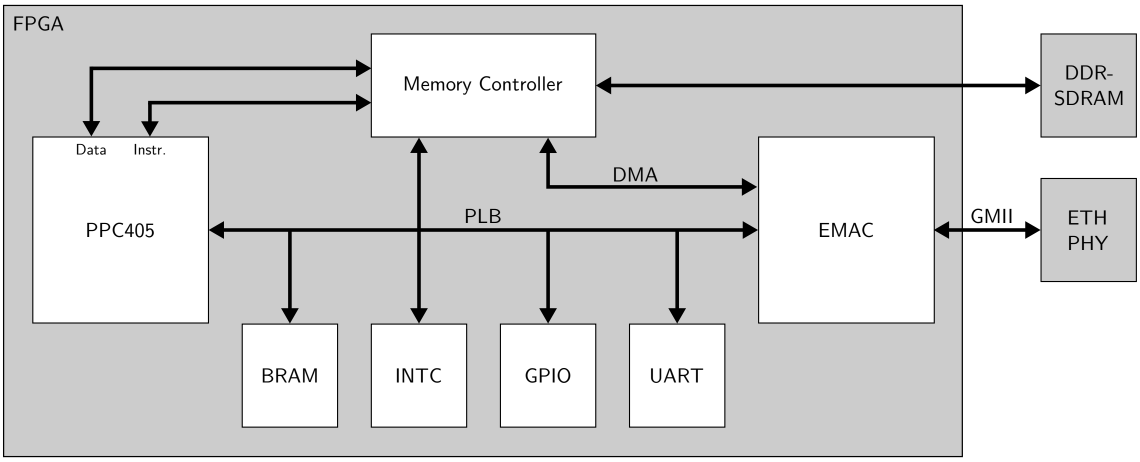

Figure 6.5: The system built to test the DDR-SDRAM is similar to the one described in Section 6.3.2 but additionally includes a memory controller to which the external DDR-SDRAM is connected. The memory controller provides four dedicated internal ports: two providing data and instructions for the PPC405, one connected to the PLB, and one for the DMA implementation of the EMAC.

Finally, a more sophisticated software was compiled, which makes use of the DMA of the EMAC to the memory controller and includes a test suite which can measure the Ethernet performance and the processor load by transmitting and receiving raw Ethernet packets. Table 6.2 shows the achieved data rate, the network utilization as fraction of the maximum effective data rate[8], and the CPU utilization (fraction of the time in which the processor is not in idle state) for different packet sizes. The packet threshold setting or DMA interrupt coalescing defines how many packets are queued in memory before an interrupt is sent to the CPU. Therefore, instead of servicing every single packet, the CPU can process a bunch of packets, thus reducing the interrupt overhead, which gets visible in the CPU utilization especially for small packets.

As it can be seen from Table 6.2, a link utilization of nearly 100 % can be achieved with medium sized frames, and by queueing packets, the CPU utilization can be reduced. At the maximum frame size defined in the Ethernet standard, the link utilization reaches 100 %, with the CPU spending time in idle state while servicing every packet. With the ‘jumbo’ frames, this situation obviously improves even more.

This test clearly shows that the implementation of the Ethernet PHY and especially of the DDR-SDRAM is working properly and reliable. The theoretical bandwidth of 6.4 $\mathrm{Gbit\,s^{-1}}$ easily outperforms the baseline implementation with one dedicated

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[8] The maximum effective data rate accounts for additional data overhead present in the Ethernet protocol which is: the preamble, the start-of-frame delimiter, and the inter-frame gap.

Table 6.2: Raw Ethernet performance and processor load using DMA for the EMAC for different frame sizes. The network utilization is the data rate fraction of the maximum effective data rate and accounts for the Ethernet packet overhead, whereas the CPU utilization is measured as the fraction of the time during which the CPU is in idle state. The packet threshold setting is a parameter of the DMA and sets the amount of packets queued in memory before an interrupt is issued to the CPU. Increasing this parameter means that instead of servicing every single packet immediately, they will be queued and processed in a burst, which reduces the processing overhead and thus the load of the processor.

	Packet Threshold settings					
	1			64		
Frame size bit	Data rate Mbps	Net Util %	CPU Util %	Data rate Mbps	Net Util %	CPU Util %
64	262.8	34.5	100	260.6	34.2	100
128	526.8	60.9	100	522.4	60.4	100
512	957.0	99.4	100	956.9	99.4	47
1518	985.7	99.9	74	985.7	99.9	16
9000	997.5	100.0	12	997.2	99.9	3

SRAM per PDM, which results in a total bandwidth of $2.56\,\mathrm{Gbit\,s^{-1}}$ for eight PDMs. Despite the fact that the achievable data rate will be lower than the theoretical one, there is enough margin to account for the refresh cycles during which the memory will be busy. In addition, the implemented DDR-SDRAM can be operated at twice the tested clock rate, which also applies to available space qualified models.[9]

6.3.4 System Monitor

As an integral part of the housekeeping, the system monitor provides all the engineering data, monitors the health of the system and generates alarms in case any parameter reaches the defined operational limits. To make sure that the implementation works reliable and can be used for EUSO-Balloon and EUSO-SPB, it was systematically tested. For that purpose, a computer software was written which provides low-level access to the MAX34441 and allows the configuration and reading of the various parameters like the setting of the voltage divider ratios, current gains,

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[9] New technology has become available which includes space qualified DDR3-SDRAM, which supports clock rates up to 667 MHz. Nevertheless, it should be stressed that the Virtex-4QV (speed grade 10) only supports DDR-SDRAM interfaces up to 213 MHz and DDR2-SDRAM interfaces up to 255 MHz (Xilinx, 2010d). This also applies to the Virtex-5QV (speed grade 1), which supports DDR-SDRAM and DDR2-SDRAM interfaces up to 200 MHz (Xilinx, 2015).

or alarm- and warning-thresholds. Additionally, the software also acts as an emulator for the HK system and provides a high-level interface that reads the engineering data and displays them in a clear way so that any parameter outside the operational range gets immediately visible.

The accuracy of the voltage, current, and temperature measurements have been validated by cross checking the readings with an oscilloscope and a multimeter. This showed that the measurements are within 1 % for voltages and currents (which is also the accuracy given in the datasheet of the MAX34441) and within a few degrees for the temperature[10]. This was regarded as accurate enough as the requirement for the supply voltage stability of the FPGA is ±5 %. Nevertheless, the MAX34441 provides enough flexibility so that any possible manufacturing variation (e.g., in the resistance of the sense- and voltage-divider resistors) can be compensated by adjusting the corresponding gain and voltage divider ratio parameters.

6.4 EUSO-Balloon & EUSO-SPB Cluster Control Board

6.4.1 Thermal-Vacuum Tests

To make sure that the electronics stay within their operational temperature range, the thermal design of the EUSO-Balloon and EUSO-SPB CCB (see Section 5.2.2) was carefully validated during several thermal-vacuum test campaigns. According to the thermal test procedure (Medina-Tanco, 2012), a thermal cycling test was defined as a result of the thermal analysis (Medina-Tanco et al., 2012). The CCB was tested throughout 2.5 thermal cycles as described in the following (a scheme is given in Figure 6.6):

1. the chamber is evacuated to $(3 \pm 2)\,\mathrm{mbar}$
2. the cycle starts with the subsystem switched on with full load at ambient temperature
3. the chamber is driven as fast as possible to $+50\,°\mathrm{C}$ but not faster than $dT/dt \approx +1.3\,°\mathrm{C}\,\mathrm{min}^{-1}$ to avoid mechanical damage
4. as soon as the temperature rise $\Delta T/dt$ is less than $0.05\,°\mathrm{C}\,\mathrm{min}^{-1}$, the subsystem is kept at $+50\,°\mathrm{C}$ for 13 h
5. after that, the chamber is driven to $-20\,°\mathrm{C}$ not faster than $dT/dt \approx -0.7\,°\mathrm{C}\,\mathrm{min}^{-1}$

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[10] Cross checking the core temperature of the FPGA is however not possible and a temperature sensor mounted on the MAX34441 package will include some error due to the thermal resistance between the interfaces of the internal sensor to the package and to the external sensor.

6. the subsystem is held at −20 °C for 13 h as soon as $\Delta T/dt < 0.05\,°\mathrm{C\,min^{-1}}$
7. the chamber is again driven to +50 °C with $dT/dt \leq +1.3\,°\mathrm{C\,min^{-1}}$, and crossing the ambient temperature defines the end of the first cycle
8. additional 1.5 cycles have to be performed, and the system is pressurized after reaching ambient temperature after the last cycle

The first test was done with the CCB mounted inside a small vacuum chamber, which was placed inside a thermal test chamber. The thermal chamber controls the air temperature in its interior and thus the skin temperature of the vacuum chamber. To account for the thermal resistance between the thermal structure of the CCB and the DP (which interfaces the radiator plate), only the cooling plate was connected to the vacuum chamber with several copper wires. Temperature sensors (Pt100) were placed on the thermal structure of the CCB, the SRAM and on a few locations on the vacuum chamber. Additionally, the air temperature of the chamber and the pressure inside the vacuum chamber were monitored.

As it can be seen from Figure 6.7, the pressure inside the vacuum chamber was at 2 mbar throughout the whole thermal cycles and thus within the requirement. As all the mounted components comply to the industrial temperature grade (−40 °C to

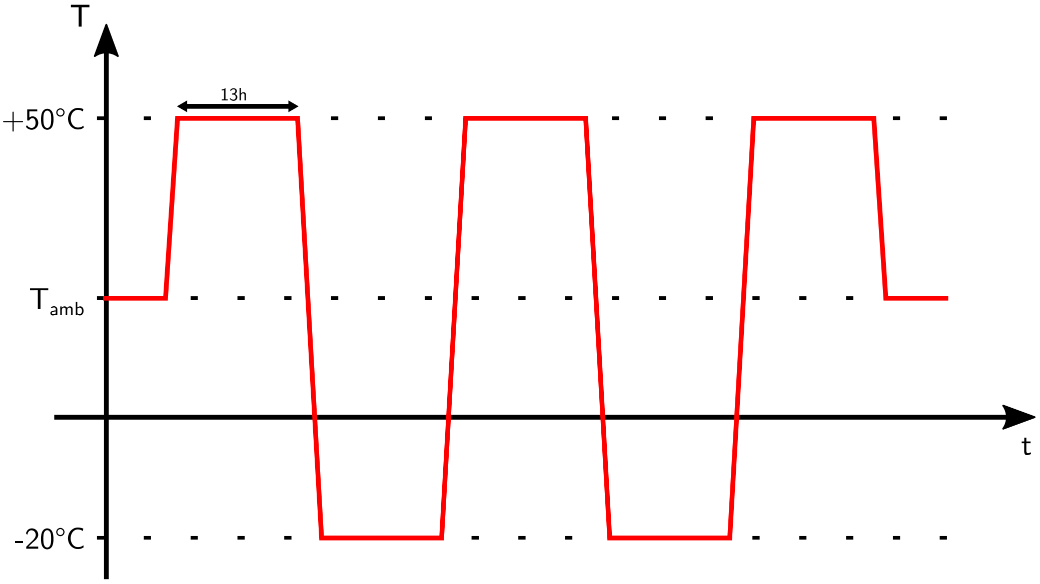

Figure 6.6: Schematic view of the thermal cycle test. The test starts and ends with the subsystem under full load at ambient temperature and a pressure of (3 ± 2) mbar. For each cycle, the temperature of the subsystem is first driven to +50 °C and then to −20 °C, while each temperature is held for at least 13 h. In total, 2.5 cycles have to be performed.

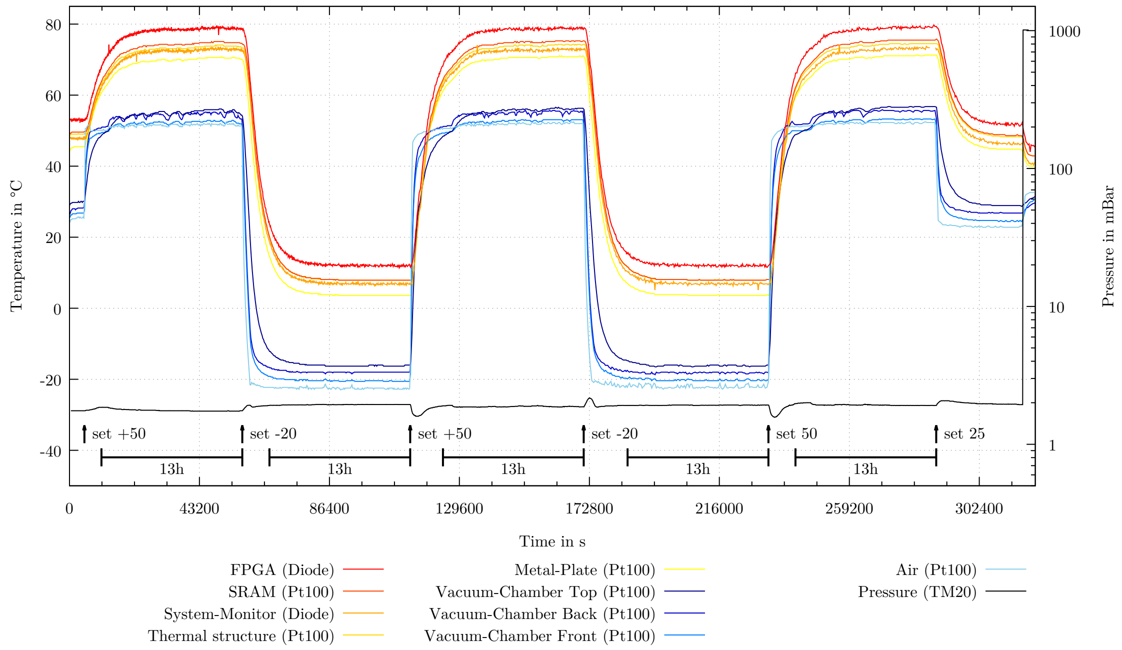

Figure 6.7: Temperatures and pressure during the thermal cycle test of the CCB. As required, the pressure was held at 2 mbar during the 2.5 cycles, so that heat transfer due to convection is prevented. Due to the low thermal resistance of the thermal structure from the CCB, the critical components stayed well inside their operational temperature range.

+80 °C), only the hot case was regarded as critical and especially the core temperature of the FPGA. With a temperature difference of 8 °C between the FPGA core and the metal plate of the thermal structure together with a power dissipation of 5.9 W, the total thermal resistance found is $R_\theta = 1.35\,\mathrm{K\,W^{-1}}$. Therefore, the FPGA stayed well below its maximum operational temperature of 100 °C even with the rather high 'artificial' thermal resistance in the interface between the thermal structure of the CCB and the radiator of around $2.5\,\mathrm{K\,W^{-1}}$ created by the copper wires. This includes enough margin for any additional thermal resistance and heat generated by other components inside the DP rack.

As part of the flight validation procedure, a system wide thermal vacuum test was required by CNES and performed using the large thermal vacuum chamber SIMulateur Environnement Opérationnel Nacelles (SIMEON) from CNES in Toulouse, France. The assembled DP and PDM were mounted in flight configuration on a metal plate which acts as the radiator for the electronic boxes. During the final instrument assembly, this metal plate will be mounted directly to the instrument radiator on top of the instrument booth. Additionally, the system was covered with thermal

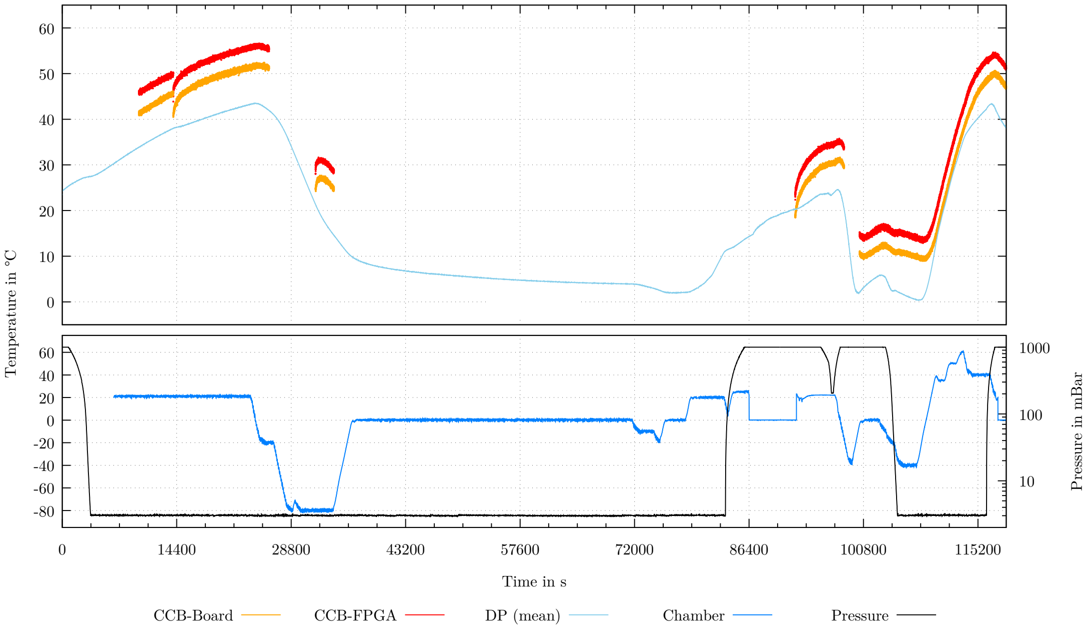

Figure 6.8: Thermal data from the CCB during the system wide thermal vacuum test. The temperature of the radiator was controlled between 0 °C to +50 °C at a pressure of 3 mbar. Due to power supply problems of the HK (at low temperatures) and the PDM (at high temperatures), the system could not be started or had to be switched off several times and thus only partial data from the internal sensors of the CCB are available. The thermal resistance found between the FPGA core and the DP structure is with $1.57\,\mathrm{K\,W^{-1}}$ only slightly larger than the one found in the thermal cycle test of the CCB. This is the result of a very good thermal contact between the thermal structures of the CCB and the DP.

insulation material such that the heat transfer was only possible via this radiator. At the time of this test campaign, the launch site and date was already fixed (Timmins, Canada, in summer) and the requirement on the operational temperature range was relaxed. Therefore, the temperature of the radiator for the electronics was controlled between 0 °C to +50 °C.

The thermal data recorded from the CCB (in particular the core temperature of the FPGA and the temperature of the board) were sent via the HK to the CPU and recorded to a file. Due to thermal issues of the power supply for the HK, it was not possible to start the HK at low temperatures. In addition, thermal problems of the PDM power supply at high temperatures and issues with the isolation of the HV associated with low pressure were found (see also Barrillon et al., 2016). Therefore, the system had to be switched off several times or could not be started and thus no continuous data are available from the internal sensors of the CCB. Nevertheless, it can be seen in Figure 6.8 that the temperature difference between the FPGA and the DP mechanical structure stays constant at around 8 °C. Together with a power dissipation of around 5.1 W, the thermal resistance between the FPGA core and the DP structure is $1.57\,\mathrm{K\,W^{-1}}$. This is only slightly larger than what was found between the FPGA core and the metal plate of the thermal structure from the CCB and indicates a very good thermal contact between this metal plate and the DP structure which is directly mounted to the radiator. In fact, a thermally conductive pad was used at this interface to keep the thermal resistance as low as possible.

6.4.2 Housekeeping flight data

The HK data related to the CCB, which were collected during the EUSO-Balloon flight is shown in Figure 6.9. As it can be seen from the temperatures, the system radiator on top of the gondola dropped during the ascent from 25 °C to −10 °C and continuously decreased during the night to −16 °C. This resulted in a temperature of the DP structure of around 30 °C at launch, dropping to 5 °C when the flight was terminated. The temperature difference between the FPGA core and the mechanical structure of the DP was at 14 °C and thus higher than in the previous tests. It should be noted, that the tests done in the SIMEON already showed a temperature difference of around 4 °C, depending on the mounting position of the sensor. However, based on the carefully designed and validated thermal structure, the CCB was operated in a convenient temperature range during the flight and could be safely operated up to a DP skin temperature of 70 °C, which exceeds the requirement by 40 %.

The power supply of the CCB provided stable voltages throughout the whole flight at a total power consumption of around 5 W. The input voltage provided by the LVPS at a nominal voltage of 5 V was with 4.8 V slightly lower due to the voltage drop in the cable and the connector, but still within the requirement of ±10 %.

The engineering data of the CCB collected during the EUSO-SPB flight are shown in Figure 6.10. Clearly visible in the thermal data is the temperature change of the instrument between night and day at its current location, which becomes even more pronounced when the balloon started to loose altitude. The temperatures of the CCB during the first few days of the flight are comparable to the ones observed during the EUSO-Balloon flight, but the instrument continued to cool down. This culminated in a huge temperature drop of nearly 40 °C when the balloon passed severe weather condition underneath, which resulted in an FPGA core temperature of −21 °C and a board temperature of −24 °C.

From the current measurement of the 2.5 V rail, a drop in the power consumption of the CCB can also be identified after a restart of the subsystems on May 1st, 2017, at 16:22 UTC (data taking phase was already finished for that night). The drop in the total power consumption is around 3.8 % and did not reappear until the termination of the flight. As it is present in the data of the LVPS as well as in the data collected

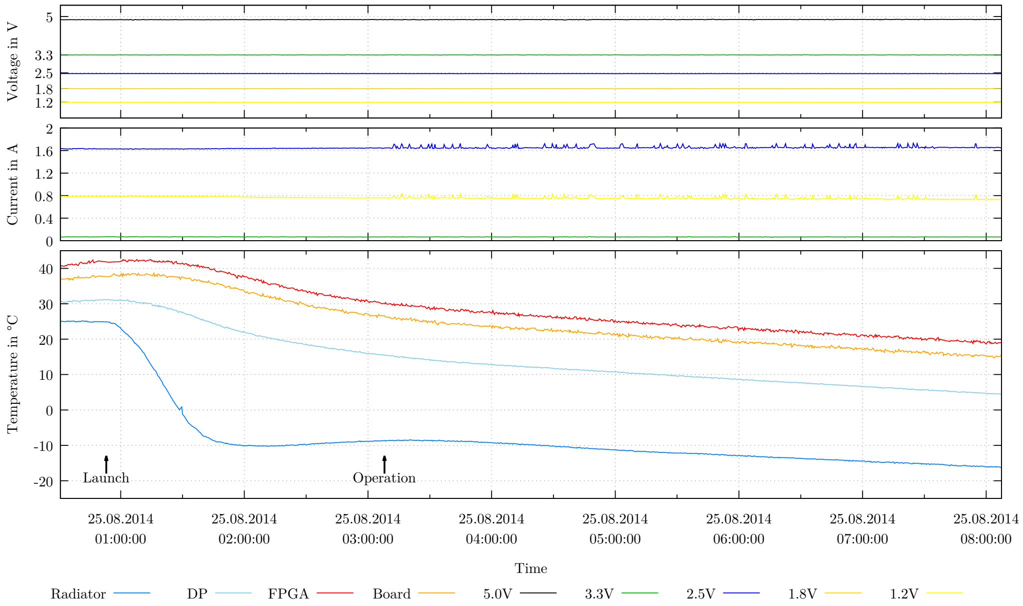

Figure 6.9: HK data of the CCB collected during the EUSO-Balloon flight. During the ascent and the night, the temperature of the main radiator dropped to −16 °C, which resulted in a continuous decrease of the FPGA temperature from 42 °C at launch time to 19 °C at flight termination. The start of the instrument operation can be clearly seen as fluctuations in the power consumption.

by the CCB, a measurement error can be excluded. Furthermore, as this reduced power consumption does not fit to any of the operational modes of the CCB and as the instrument was apparently operating as usual, the reason for this reduced power consumption is still unclear and under investigation.

A close look at the different voltage rails reveals a very small variation of the voltages over a temperature range from −24 °C to +30 °C. The total change is between +0.1 % for the 1.8 V rail and +0.4 % for the 2.5 V and is well within the requirement of ±5 %. This temperature dependent change in the measured voltages is the result of a combination of the typical temperature variation of the regulators (±0.5 %), the temperature drift of the ADC reference (±0.5 %), and the temperature coefficient of resistors ±0.02 % used for feedback or voltage dividers. Therefore, this variation is the result of a combination of temperature dependent voltage generation and measurement.

6.4.3 L2 Trigger Performance

In order to prove the functionality of the CCB during the development process and to verify the correct behavior including its interfaces and the interaction with the

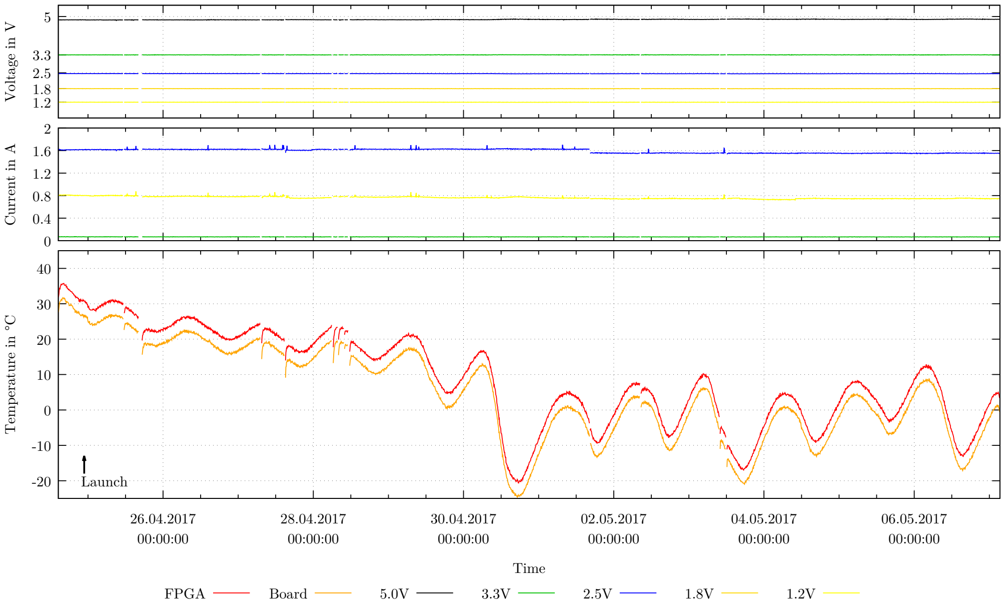

Figure 6.10: HK data of the CCB collected during the EUSO-SPB flight. The temperature change of the instrument between night and day is clearly visible in the CCB temperature data, together with a steady cooling down during the first few days at float altitude. On April 30th, the instrument passed over a thunderstorm, which resulted in very low temperatures of the instrument, and the core temperature of the FPGA reached −21 °C. The reason for the drop in the power consumption of the CCB, which is visible in the current data from the 2.5 V rail, is unclear and still under investigation.

other modules, several test-setups were developed.

A first test of the hardware implementation of the L2 trigger algorithm was successfully performed with simulated data which were processed by the FPGA but did not include a test of the interfaces. By comparing the results of this self-contained test environment with software simulations, it was shown, that the implementation is working correctly and only minor differences were found which had no influence on the overall trigger efficiency (see Bayer, 2011; Bayer et al., 2011).

For a more advanced validation of the CCB, a stand-alone 'PDM-Simulator' was developed (Gottschall, 2013) and used to verify the overall functionality including the interface between the CCB and the PDM. The 'PDM-Simulator' is based on a Spartan-3 FPGA and receives simulated events generated in the 'EUSO Simulation and Analysis Framework (ESAF)'. When a complete event is stored inside the 'PDM-Simulator', it generates an L1 trigger and sends the event data to the CCB via the PDM interface where they are processed. In the case that an L2 trigger is issued, the event is transferred to a computer via a SpaceWire interface and analyzed further with the 'Near Real Time Analysis (NRTA)' software. This software was specifically developed for the project as part of the GSE and allows a first quick look into the received data during the balloon flights (see Wille, 2017). To include all interfaces of the CCB in the verification process, the 'PDM-Simulator' also provides the system- and GTU-clock and an additional 'HK-Simulator' – based on an MCU – simulates the interface towards the HK system and allows the collection and display of the engineering data (see also Bayer et al., 2013). This hardware test-bench was extensively used to improve, optimize and validate the functionality of the CCB in the laboratory, and in the field with the prototype CCB which was successfully integrated and tested in the EUSO-TA instrument.

In addition to the validation of the general functionality, this test-bench was also used to demonstrate the performance of the L2 trigger algorithm and especially, to demonstrate that the overall processing time is only around 5.7 ms. In particular, the decision, whether to issue an L2 trigger or not, is done before all data are received from the PDM. This is possible because the evaluation of the trigger algorithm is only depending on a small fraction of the complete data frame – to be precise, only 29 GTUs out of 128 GTUs are needed – and the evaluation starts as soon as all necessary data are received. In addition, the implementation of the L1 trigger algorithm issues the trigger around GTU number 40 within the 128 GTU frame, therefore around 60 GTUs still have to be transferred to the CCB when the final direction integration starts (see also Section 5.2.3). As the PDM interface is running at 40 MHz, it takes around 3.9 ms to transfer the remaining 60 GTUs. The L2 trigger algorithm on the other hand is running at 100 MHz and therefore, it takes only 3.8 ms to finish the 25125 integrations (375 starting points and 67 directions over ±7 GTUs). Therefore, the requirement on the L2 processing time is exceeded by a factor of more than 25, and even more important, no additional dead time is added by the L2 trigger algorithm. This is also reflected in the dead time measurement during the EUSO-SPB flight which was around 26 ms. This time is basically fixed by the data transfer times from the PDM to the CCB (around 8 ms) on the one hand, and from the CCB to the CPU (around 17 ms) on the other hand (see Scotti et al., 2019, for more details).

6.5 EUSO-SPB Photo-Detector Module Control Board

6.5.1 FPGA Configuration

In addition to the configuration interfaces available for the Virtex-4 (see Section 6.2), the Virtex-6 supports two more interfaces which can be used to attach either an industry standard SPI flash PROM or an industry standard parallel NOR flash PROM via the Byte-wide Peripheral Interface (BPI). As the EUSO-Balloon PDM control board already implemented the BPI, the layout was only slightly changed to support a different flash PROM, as the originally implemented one had been discontinued. Therefore, the working principle of the configuration interface was already tested and validated thoroughly during the EUSO-Balloon campaign and thus only the changes in the layout and the timings of the new memory had to be tested and evaluated.

Similar to the timing analysis done for the CCB, the maximum clock rate for the configuration interface can be calculated from the clock-to-data-valid delay (T_{CHQV}) of the PROM (Numonyx, 2010) and the data setup requirement (T_{BPIDCC}) of the FPGA (Xilinx, 2013)

$$T_{CYC} = T_{KHQV} + T_{BPIDCC} = 17\,\mathrm{ns} + 4\,\mathrm{ns} = 21\,\mathrm{ns},$$

which does not violate the minimum clock period requirement of the PROM, which is

$$T_{CLK,min} = 19.2\,\mathrm{ns}\,.$$

Including the frequency tolerance of the internal RC-oscillator which is given by 55 %, leads to a maximum frequency of $f_{config} = 30.72\,\mathrm{MHz}$. Configuring the RC-oscillator to $f_{RC} = 26\,\mathrm{MHz}$, which is the closest available setting, actually resulted in a generated frequency of 26 MHz for the mounted FPGA and was used to validate the configuration interface. At this frequency, the total configuration time is only 231 ms.

6.5.2 Thermal-Vacuum Tests

Similar to the thermal-vacuum tests done for EUSO-Balloon, another test campaign was scheduled also for the EUSO-SPB instrument at the same SIMEON facility from CNES. As several components (e.g., the CCB) were reused without any modification, the focus for this test campaign were the new or redesigned components like the PDM control board. Due to the very good performance of the thermal structure from the CCB, a similar one was designed for the PDM (see Section 5.3.3). As the PDM is mounted on a translation stage to adjust the focus when switching between the two- and three-lens design, the thermal coupling to the main radiator needed to be flexible. This requirement was fulfilled by establishing the thermal contact with several thick copper wires. As a similar coupling was used to introduce an artificial thermal resistance between the CCB and the 'radiator' during the thermal cycling test (see Section 6.4.1), the thermal resistance was already known and the necessary amount of copper wires could be estimated.

Unfortunately, due to technical problems of the thermal sensors which were mounted on the cooling structure of the PDM and the thermal braid, no data are available from these sensors. Thus, the final thermal resistance between the FPGA core and the radiator could not be measured exactly. In addition, the new HK was

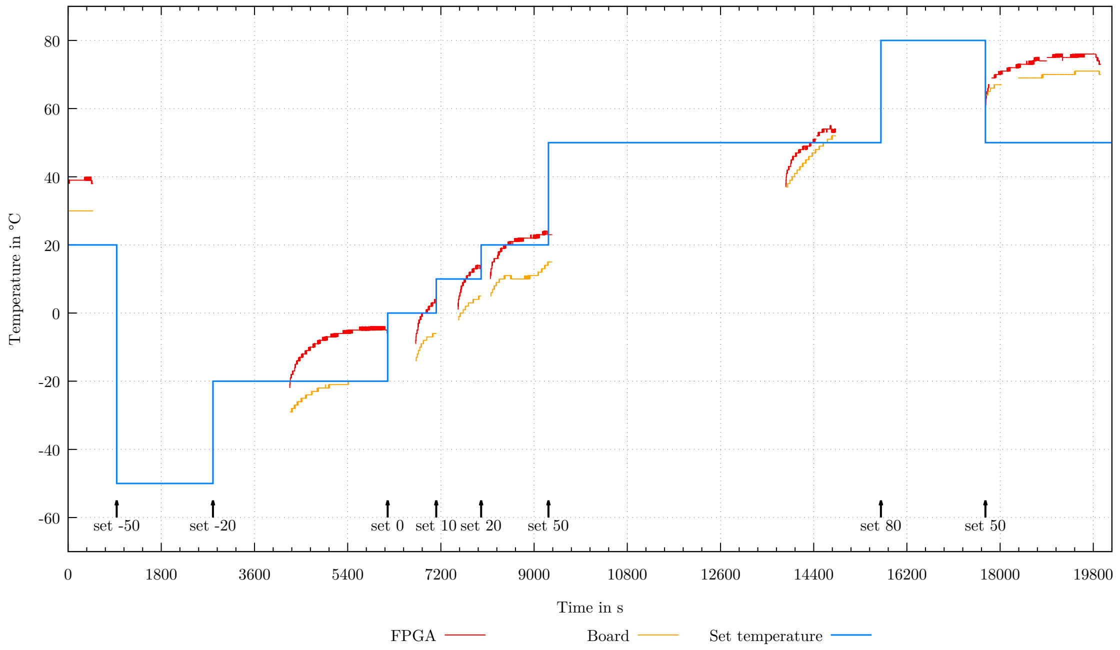

Figure 6.11: Temperature data collected by the PDM control board during the thermal vacuum tests at SIMEON for the EUSO-SPB electronics. Due to technical problems, only the internal temperatures of the PDM control board are available. As it can be seen, the PDM control board was operated between −30 °C to +60 °C without any issues, which exceeds the requirement of −20 °C to 50 °C.

not advanced enough to collect the relevant data from the instrument and only the internal data from the PDM control board could be collected via a simple HK emulator which was developed to simplify the integration between the CCB, the PDM control board, and the HK.

Nevertheless, from the set-point temperature of the chamber and from the very first temperatures recorded by the PDM after switching on, the temperature difference between the FPGA core and the radiator can be estimated to be around 20 °C to 25 °C. Together with a total power dissipation of the FPGA of around 3.5 W this leads to a thermal resistance of around $5.7\,\mathrm{K\,W^{-1}}$ to $7.1\,\mathrm{K\,W^{-1}}$. This is obviously higher than what was found for the CCB, but still a very good value, especially when taking into account that this interface is flexible and the position of the whole PDM can be changed within a certain range. This means that the PDM control board could be operated up to a skin temperature of 65 °C (and more) of the electronics radiator without overheating. In particular, it can be seen from Figure 6.11 that the PDM was successfully operated at temperatures between −30 °C to +60 °C, thus exceeding the requirement of −20 °C to 50 °C for the radiator temperature range. Therefore, the new thermal architecture was validated and the issues associated with overheating components found in the EUSO-Balloon PDM control board were successfully solved.

6.5.3 Housekeeping flight data

Given in Figure 6.12 are the HK data related to the PDM control board which were collected during the EUSO-SPB flight. Due to the lower power dissipation of the FPGA but higher thermal resistance between the FPGA core and the electronics radiator, the temperatures recorded during the flight are comparable to the ones from the CCB (see Figure 6.10). The lowest temperature (reached during the overflight of the severe weather condition) was −20 °C for the board and −9 °C for the FPGA core, while the hottest temperature was reached during the final health tests inside the hangar before launch.

The new design of the power supply was working without any issues and provided stable and clean voltages for the PDM control board and the ASIC boards throughout the whole flight. The correlation between temperature and the current measurement present in the 1.0 V rail (also slightly present in the other voltage rails) is expected and can be explained with the temperature coefficient of the current sense resistor (see also Section 6.4.2).

6.5.4 L1 Trigger Performance

The L1 trigger algorithm plays an essential role in the overall trigger and read-out scheme (see 2.4) and has to reduce the trigger rate by five orders in magnitude. The algorithm was thoroughly tested in simulations (see Fenu, 2008), and a first implementation in VHDL was validated with artificial data, generated in the rotating environment at TurLab[11], which mimics the JEM-EUSO orbit to simulate different light signatures and backgrounds by means of controlled light sources and different reflective surfaces passing underneath the detector (see for example: Bertaina et al., 2016; Miyamoto et al., 2017; Suino et al., 2017). In addition, the algorithm was tested offline with the data recorded during the EUSO-Balloon flight (see Suino et al., 2015).

In order to be able to implement this algorithm inside the FPGA of the PDM, it had to be optimized such that the necessary amount of logic resources[12] does not exceed

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[11] TurLab is facility which contains a large rotating tank with a diameter of 5 m, which can be controlled at speeds between 0.05 U/ min to 20 U/ min and is mainly uses to study fluid-dynamics.

[12] The amount of resources needed for this first implementation of the trigger algorithm is around 7 % per EC of the available resources from the XC6VLX240T which was used on the PDM of EUSO-Balloon. This means more than 60 % is necessary to implement the trigger algorithm for 9 ECs, which is not feasible especially as resources needed for additional logic is not included.

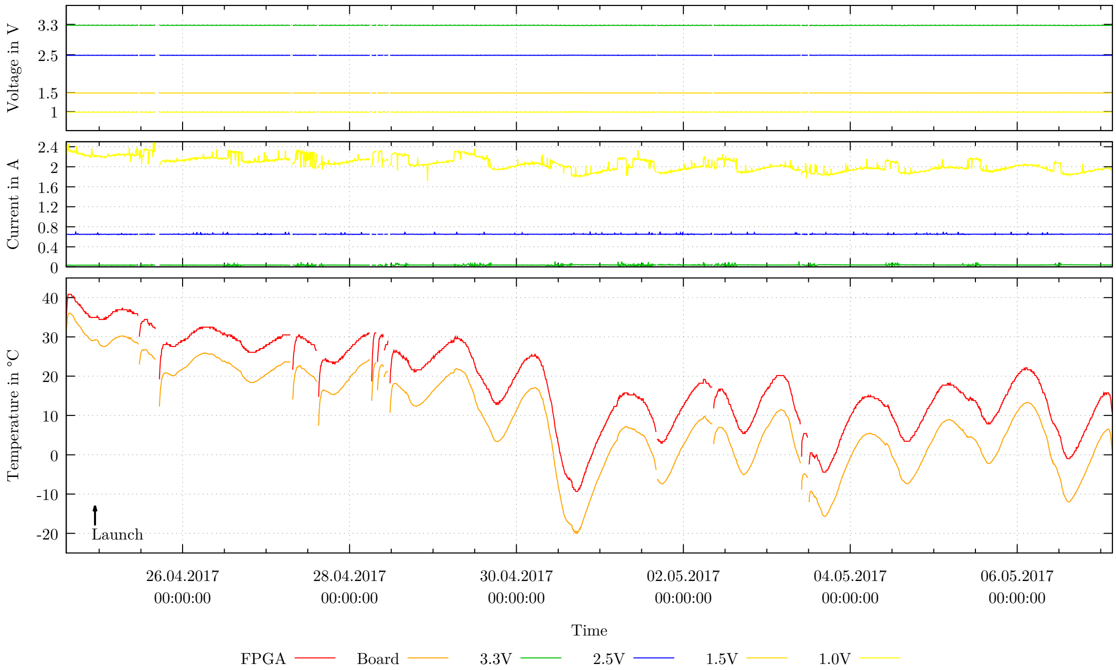

Figure 6.12: HK data of the PDM collected during the EUSO-SPB flight. The features present in the temperature data and the actual temperatures are comparable to the CCB data (see Figure 6.10). Due to the temperature coefficient of the current sense resistor, a correlation between temperature and measured current is clearly visible in the data from the 1.0 V rail.

the available resources of the FPGA, which also includes additional functionalities needed for controlling and monitoring purposes. The main part of the optimization was done by means of two different approaches:

1. the algorithm was adapted to the specific architecture of the FPGA in order to use the available resources more efficiently, and
2. by doubling the internal processing frequency, which allowed to move away from a completely parallel architecture to one in which part of the processing is done serially.

The success of these approaches can be clearly seen for example in a reduction of the used BRAMs by around 85 %. As the BRAMs are also needed to implement the 128 GTU large ring-buffers, this reduction makes the implementation of the double buffer feasible for both FPGAs (both models contain the same amount of BRAMs). The optimized trigger implementation for all 9 ECs uses 29 % of the LUTs and 14 % of the slice registers available in the XC6VLX365T used for the EUSO-SPB

PDM. In comparison, this corresponds to 43 % of the LUTs and 21 % of the slice registers available in the XC6VLX240T. The final implementation for EUSO-SPB – including the ring-buffers, all the control and monitor logic, and even additional functionalities not available during the EUSO-Balloon flight – uses around 34 % to 43 % of the available resources. The exact value depends on the type of resource considered and more details can can be found in Baehr, 2017 and Bayer et al., 2017.

6.5.4.1 Test Campaign in Utah

During the field test campaign at the TA site in Utah, USA, the fully assembled instrument was tested and calibrated by means of various light sources (see also Section 4.3). Especially the L1 trigger performance and its efficiency have been evaluated and validated with the GLS and the CLF.

With the baseline L1 trigger parameters for EUSO-SPB, $P = 1$ and $R = 1$ (see Section 2.4.1), the trigger rate during normal sky conditions was below 1 Hz – the requirement for JEM-EUSO is to keep the trigger rate below 7 Hz. During a thunderstorm (outside the FoV) or the passage of airplanes, the trigger rate increased to a few Hz. The reason for this is that during the decay of the light pulse, there is always a phase during which the amount of light is just at the edge of the trigger threshold. Due to this, the threshold N_{GTU}^{thr} was not reached in some cases and thus these events were not always discriminated as slow events and an L1 trigger was generated. The same issue also occurred rarely from time to time when a star or a meteor was crossing the border between two MAPMTs and the light was scattered sporadically by the filters into the next MAPMT. Nevertheless, the fact that the L1 algorithm did not trigger on stars under normal conditions proved that the algorithm is capable of dealing with slow events, and even under these special conditions, the trigger rate stayed below a few Hz.

To estimate the energy threshold of the instrument, the GLS – located at a distance of 24 km from the instrument – produced shower-like signals with varying energy between 0.5 mJ to 4 mJ, which where shot at an angle of 45° away from the instrument. The amount of triggered events out of the total number of shot laser pulses (100 per energy step) defines the efficiency. This measurement was done for the two different lens configurations (see Section 4.2.3) on two different nights, as changing the lens configuration had to be done during daylight. Nevertheless, to avoid systematic effects in the comparison, the sky conditions were monitored and found to be similar during the two measurements (see Eser, 2018, for more details). As it can bee seen in Figure 6.13, the detection threshold for the 3-lens configuration is more than a factor of two higher in energy. By comparing the detected laser signal to expectations from EAS simulations, the threshold energy for a 50 % trigger efficiency of the 2-lens configuration corresponds to an EAS with an energy of around 3×10^{18} eV observed

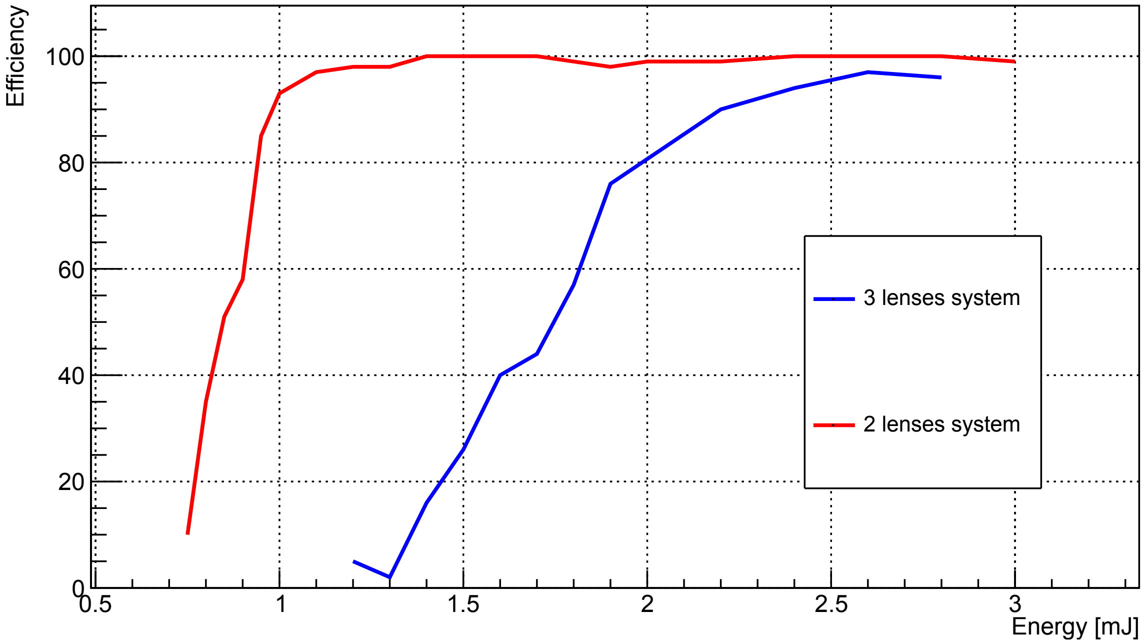

Figure 6.13: Comparison of the trigger efficiency for the 2-lens and 3-lens configuration as a function of the laser energy from shots of the GLS during the field test campaign at the TA site in Utah, USA. (Image adapted from: Bayer et al., 2017)

from a distance of 33 km at an inclination[13] of 53°.

A reprocessing of the collected trigger efficiency data was performed offline by applying the same trigger logic (see Battisti et al., 2018). A comparison of the online and offline trigger efficiency is given in Figure 6.14, which shows good agreement in the performance of the hardware and software implementation of the L1 trigger. The slightly lower trigger efficiency from the offline reprocessing at low energies is due to the fact that in the automatic mode, the trigger thresholds N and S are set according to the background value which is calculated and updated every 128 GTUs. For the offline reprocessing, these data is not available and therefore, the background estimation is done on the previously triggered data. But as the triggered data obviously contains some excess above the background, this estimate is biased. This can lead to slightly higher trigger thresholds and therefore to a slightly lower trigger efficiency. Nevertheless, this important result confirms the correct behavior of the hardware.

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[13] While the GLS was shooting the laser with an inclination of only 45°, the instrument itself was tilted by 7.8° towards the sky. Therefore, the resulting inclination of the observed laser pulse is 52.8°.

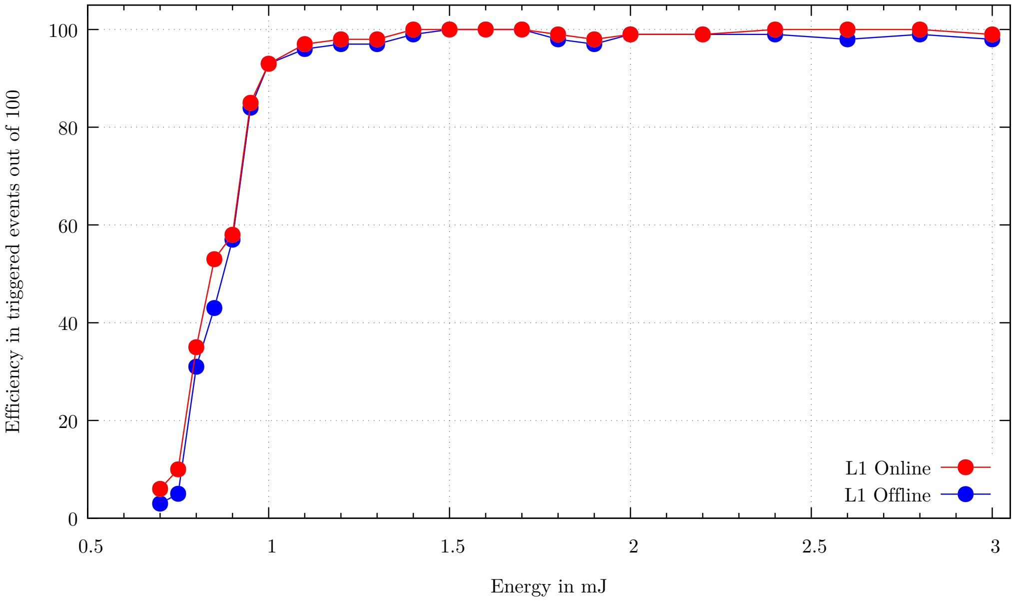

Figure 6.14: The trigger efficiency as measured for the 2-lens configuration during the field test campaign at the TA site in Utah, USA, (in red) in comparison to an offline trigger evaluation (in blue). The good agreement confirms the correct behavior of the hardware. (Plot reproduced from: Battisti et al., 2018)

6.5.4.2 EUSO-SPB flight

The overall trigger rate during the EUSO-SPB flight is given in Figure 6.15 together with the average count rate. During the first three nights, the trigger parameters were set to $P = 0$ and $R = 0$, which was expected to be the most efficient configuration for the detection of EASs for EUSO-SPB. The trigger rate was around 1 Hz per EC, which was above the trigger rate imposed by the downlink telemetry constraints. Therefore, the parameters were adjusted to $P = 1$ and $R = 1$, which reduced the trigger rate to less then 2 Hz for the complete PDM. These parameters were kept throughout the rest of the flight except for one night in which the most suitable settings for JEM-EUSO ($P = 4$ and $R = 2$) was tested. The peaks in the trigger rates are often related to electronic disturbances in one specific EC and are still under investigation. Some of the high trigger rates, especially the ones which started to appear from April 30th on, can be explained by interference between the health LED (see Section 4.2.4.3) and the aviation transponder, which had to be activated as soon as the altitude of EUSO-SPB dropped below 20 km. The high transmission power of this transponder triggered the health LED at high frequency which in turn triggered the instrument. In order to mitigate this problem, the health LED had to be switched off as soon as the transponder was activated. The variability in the count rates are

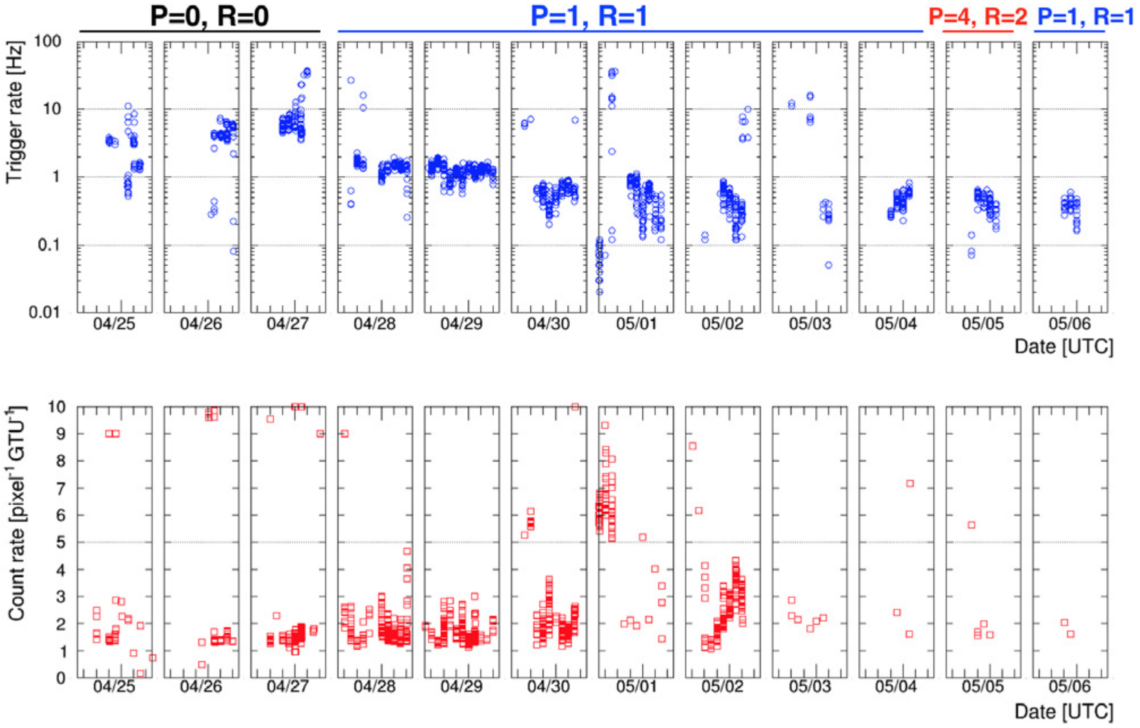

Figure 6.15: Trigger rate during the EUSO-SPB flight (top) and the average count rate at pixel level (bottom). The trigger parameter setting which was used during the different nights in 2017 is indicated on the top. (Image: Bayer et al., 2017)

due to different atmospheric conditions and the presence of moonlight.

In general, the trigger rate was below the 7 Hz requirement for JEM-EUSO but typically higher than the expectations from the measurements on ground. The ongoing analysis of the downloaded data indicate that the vast majority of the triggered events are presumably due to direct hits of CR, which still has to be confirmed by simulations.

6.5.5 High Voltage Switching Algorithm

During the integration in Golden (Colorado, USA), an end-to-end test of the implementation of the HV switching algorithm (see Section 5.3.1) was performed. An LED with adjustable intensity was set up in front of the detector and produced light pulses with a fixed duration of 10 GTUs (250 µs). While the HVPS provides an interface to independently increase the HV of the photocathode at the level of one EC, the algorithm itself monitors the light intensity of every single pixel. Therefore, a mask was installed in front of the detector in order to validate the correct behavior of the algorithm in case a single pixel receives too much illumination.

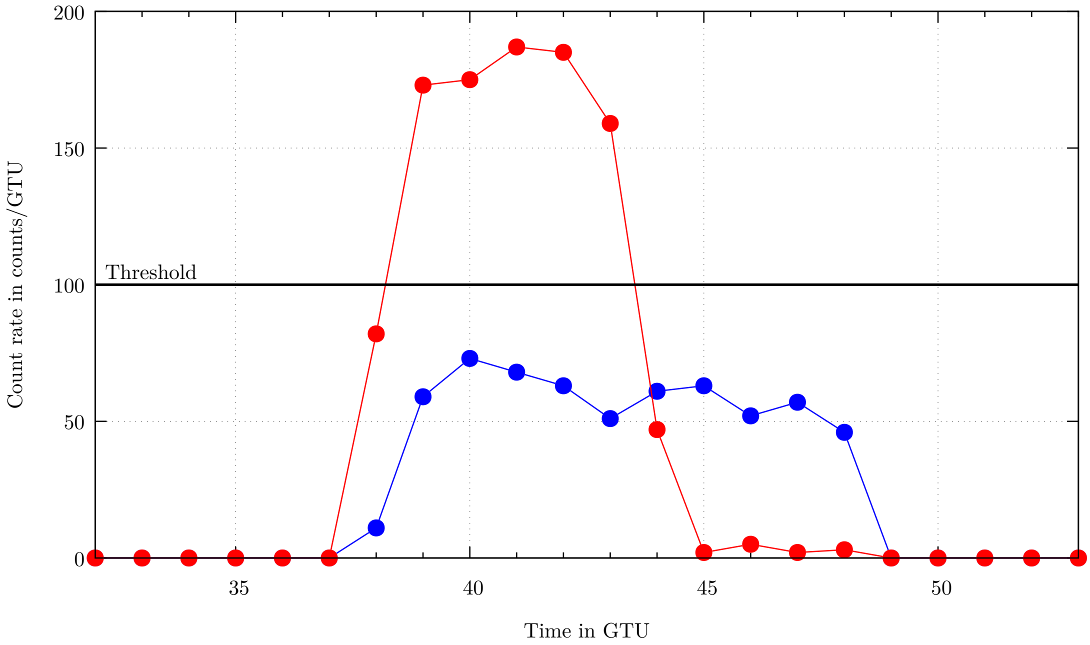

Figure 6.16: Testing of the HV switching algorithm during the integration. An LED produced light pulses with a duration of 10 GTUs and different intensities, which illuminated a single MAPMT channel selected by means of a mask in front of the detector. The data shows the light curves of two different LED pulses as a function of the GTU time inside the triggered event, which are overlayed on top of each other. The intensity of the LED pulse shown in blue was below the threshold (set to 100 counts per GTU) and thus did not trigger the algorithm. Whereas the intensity of the LED pulse shown in red exceeded the threshold and triggered an increase in the voltage of the photocathode, which results in just a few recorded counts during the remaining part of the light pulse (GTU 44 to 48).

Shown in Figure 6.16 are the superimposed light curves of two LED pulses with different intensities as a function of the relative GTU inside the recorded packet (the L1 trigger position inside the ring-buffer corresponds to GTU number 38). The light curve in blue shows a light pulse with an intensity of around 60 counts per GTU which was below the threshold to trigger the increase of the photocathode voltage. The intensity for the second light pulse (shown in red) was increased to around 180 counts per GTU and thus, at GTU number 39, it exceeded the threshold which was set to 100 counts per GTU for this test. Four GTUs later, the change in the voltage of the photocathode becomes active, and the count rate drops to around 3 counts per GTU for the remaining duration of the LED pulse.

It should be stressed that the evaluation of the algorithm happens within one GTU but it takes a few GTUs until the new setting is active at the HVPS. In case of a positive evaluation, the timing is as follows:

- *GTU 0:* the photon counting data are recorded by the ASICs,
- *GTU 1:* the data are sent to the PDM, are analyzed, and the algorithm is evaluated,
- *GTU 2:* the new setting for the voltage of the MAPMT photocathode is sent to the HVPS control board via a serial interface,
- *GTU 3:* finally, during the following GTUs, the new voltage is applied to the photocathode by the activated switches of the HVPS.

6.6 EUSO-Balloon

The results which are presented in this section (as well as Section 6.7) have either been obtained by the entire collaboration or are the results of different data analyses and are not a part of this work. Thus, they are only briefly described. More information about the results of the balloon flights can be found for example in Abdellaoui et al., 2019; Bertaina, 2019 and Abdellaoui et al., 2018.

6.6.1 UV Background

The amount of diffuse light, arising form natural and artificial light sources, increases the noise level of the instrument. This is simply because the light of the UHECR events has to be significantly brighter than this background in order to be detectable. The exact amount of background light is important to know, as it affects the trigger efficiency on the one hand, and introduces errors in the data analysis on the other hand. Compared to previous measurements of the diffuse UV background, a major difference is that EUSO-Balloon is an imaging instrument with a spatial resolution of around 130 m on ground. Therefore, the measurement of the diffuse UV background was a B-level requirement for EUSO-Balloon (see Section 3.2.2).

Two example pictures from EUSO-Balloon are shown in Fig. 6.17. For both pictures, the average of the counts within one data packet (128 GTUs or 320 µs) was taken. At the time of the first data packet, the instrument was above the eastern part of Timmins and several artificial light sources from a mining area are visible. The second packet was taken roughly 2.5 h later when the instrument was above forest and thus it is not expected to contain any significant artificial light sources (see Abdellaoui et al., 2019). The time of the packet, the current ground position of the optical axis, the height, and the orientation of the instrument are given at the top of the pictures.

The time evolution of the averaged, normalized count rates during the Time interval Of Interest (ToI) is shown in Fig. 6.18. The ToI starts at 03:08 UTC after

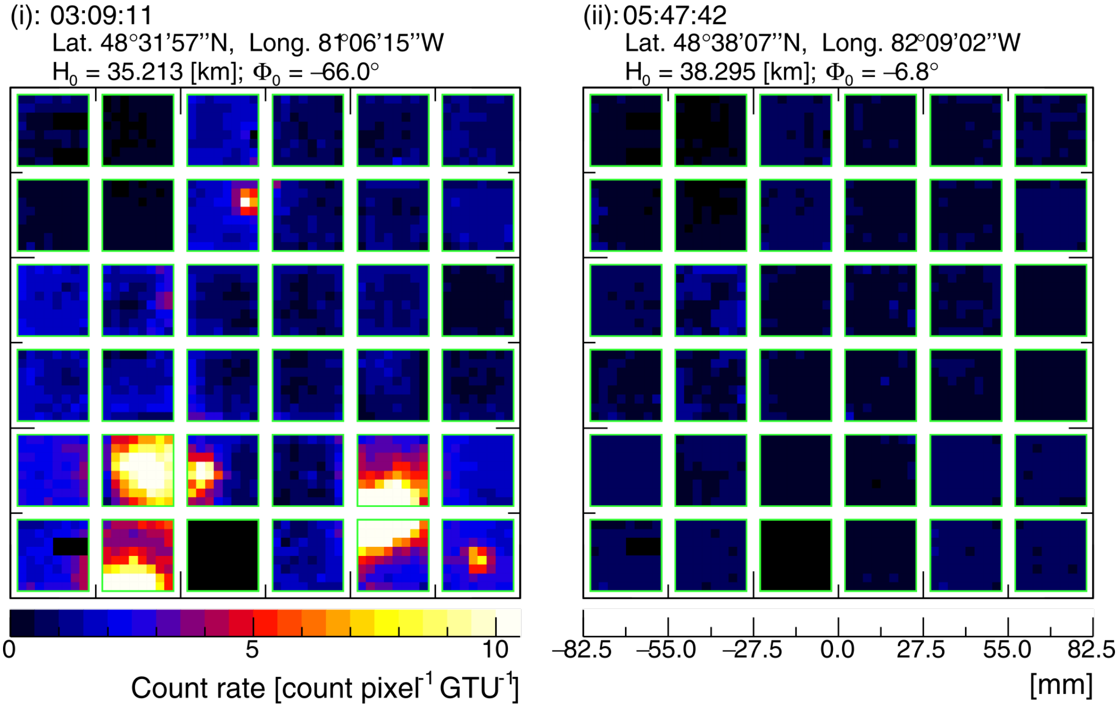

Figure 6.17: Example pictures from the EUSO-Balloon PDM which show the average of one data packet (128 GTUs). While in the first picture from 03:09:11 UTC several bright spots from a mining area are visible, the second picture contains no significant artificial light sources as the instrument was above forest during that time. (Image: Abdellaoui et al., 2019)

the astronomical twilight and ends at 05:48 UTC when various engineering test were performed. The normalized count rates takes the efficiency of the single pixels into account which was obtained during the absolute calibration. Compared to JEM-EUSO, the flight altitude of EUSO-Balloon is low and thus only the back-scattered light of the airglow – which is produced at altitudes between 85 km to 300 km (see Section 2.1) – and back-scattered light from extraterrestrial sources contribute to the measured diffuse light. As the reflectivity of clouds is higher compared to forest, the time window with the lowest counts (between 04:38 UTC and 04:52 UTC) is expected to be associated with a clear atmosphere. During this time window, the mode of the distribution of the averaged normalized count rates is $\hat{N}_0 \approx 0.65\,\mathrm{pe\,pixel^{-1}\,GTU^{-1}}$. With ray trace simulations, the response of the optics can be taken into account, and this value can be converted to an absolute intensity of $I_0 = 300 - 320\,\mathrm{photons\,m^{-2}\,sr^{-1}\,ns^{-1}}$ in the 300 nm to 500 nm band (Abdellaoui et al., 2019). Despite the fact that the values are difficult to compare between different experiments due to the large variability (seasonal, daily and more frequent) the obtained values are in good agreement with previous measurements.

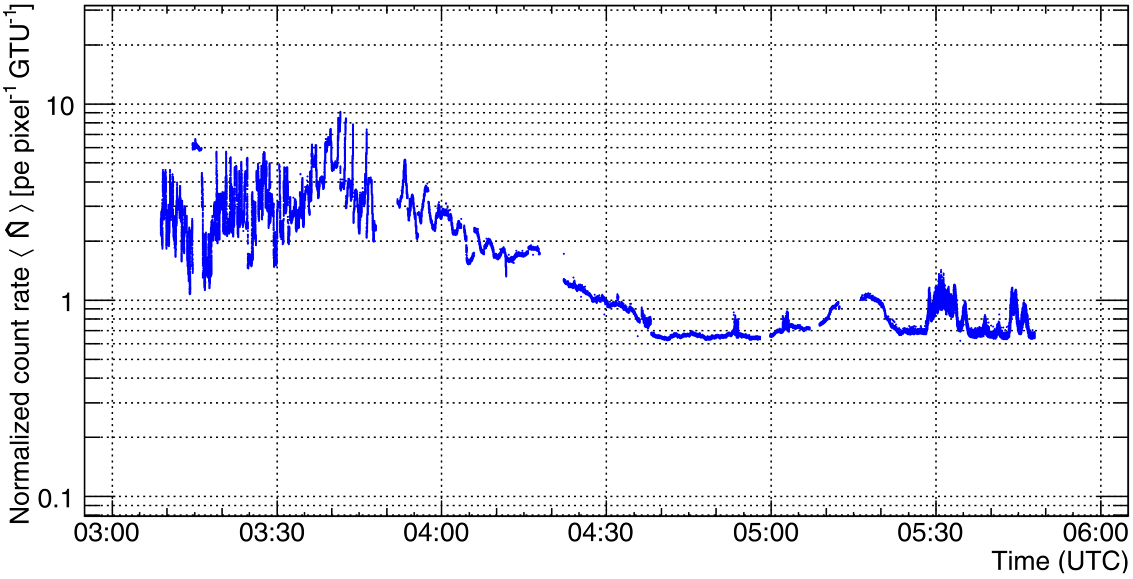

Figure 6.18: The averaged (over one packet), normalized count rates, as a function of the packet time. The breaks in data are due to temporary hardware problems and foreseen technological tests. (Image: Abdellaoui et al., 2019)

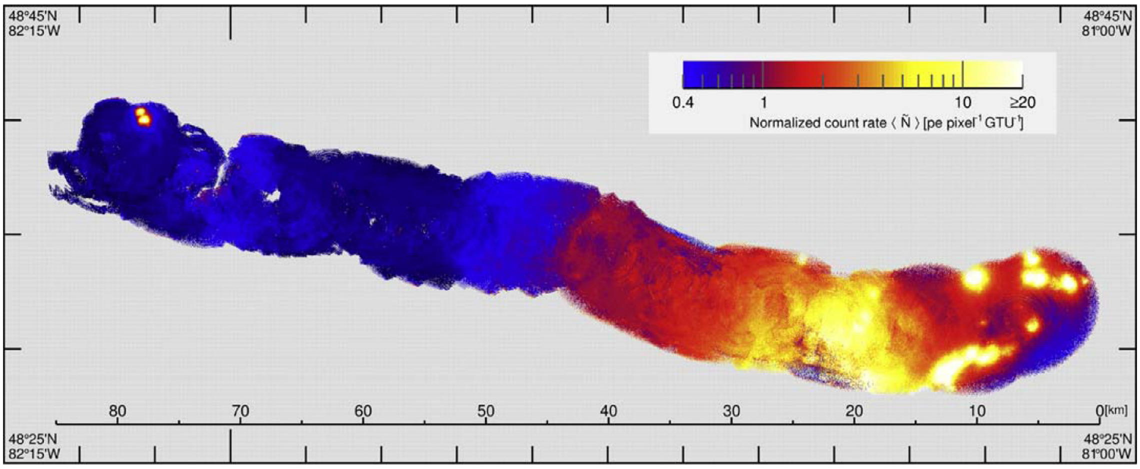

Figure 6.19: UV map obtained by EUSO-Balloon. This map shows the averaged normalized count rates mapped to geographic coordinates (no values are determined in the gray area). (Image: Abdellaoui et al., 2019)

By projecting the averaged normalized count rates onto geographic coordinates, the UV map which is given in Fig. 6.19 is obtained. With the help of map services and Landsat imagery, several ‘hot spots’ have been identified as ground facilities like the airport, factories, and mines. This demonstrates clearly the imaging capabilities of the EUSO-Balloon instrument with its wide FoV and large aperture refractive Fresnel optics. More details on the data analysis of EUSO-Balloon are given in Abdellaoui et al., 2019.

6.6.2 Angular Resolution

During the first part of the EUSO-Balloon flight, a helicopter equipped with different light sources, generated artificial EAS events (see also Section 3.4). By reconstructing the zenith angle of the recorded laser events, these data were used to estimate the quality of the direction reconstruction of the EAS.

The mean of the distribution of the reconstructed zenith angles was found to be at $(92.2 \pm 3.8)°$. As the helicopter was flying in circles and thus was slightly tilted by around 1-2°, the mean of the distribution is also expected to be slightly larger than 90°.

While the requirement for the arrival direction determination of JEM-EUSO was not reached ($\leq 2.5°$ for $E = 10^{20}$ eV, see Table 2.1), this is a very promising result as the angular resolution of EUSO-Balloon was expected to be slightly worse. This is based on the duration of one GTU, which was optimized for JEM-EUSO and should be shorter for EUSO-Balloon due to its smaller distance to the EAS. More details regarding the angular reconstruction can be found in Eser, 2018 and Abdellaoui et al., 2018.

6.7 EUSO-SPB

The EUSO-SPB instrument was operating for 292 h, during which it recorded data for a total of around 40 h during the night (see also Section 4.4). The collaboration’s analyses of the data, which was downloaded before the splash-down, is ongoing and several events with a track-like structure have been found – two example events are shown in Fig. 6.20. As the majority of these events only last for 1-2 GTUs, it is assumed that these events originate form CRs which directly hit the detector (e.g., the filter or the MAPMT). Post-flight simulations indicate that around 1 EAS event is expected in the available data sample, however, no EAS event has been identified up to now (Bertaina, 2019).

To estimate the angular resolution of the EUSO-SPB instrument, a similar analysis as it was done for EUSO-Balloon was carried out by the collaboration. Due to the early termination of the flight, the planed aircraft under flight had been canceled.

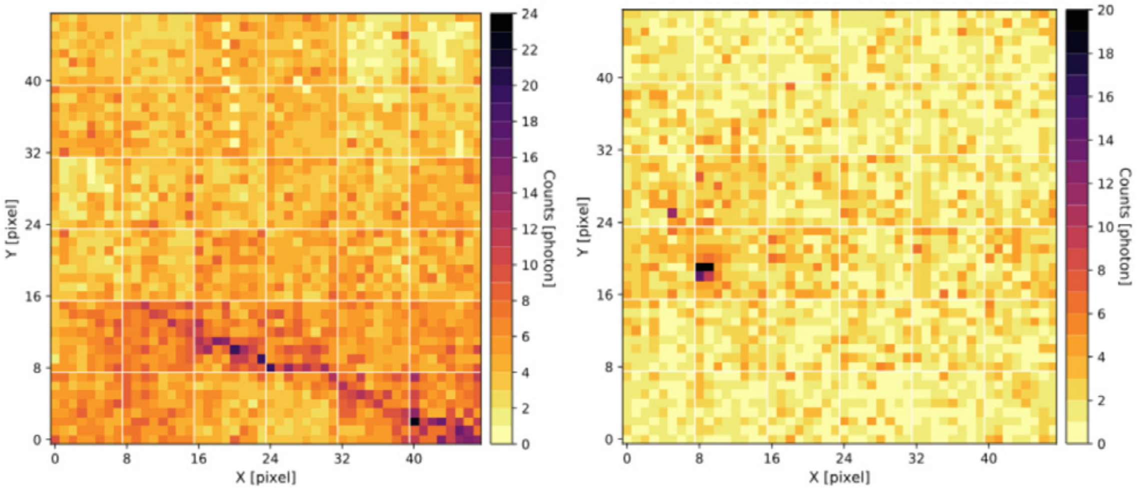

Figure 6.20: A track (left) and a 'blob' (right) which triggered the L1 algorithm during the EUSO-SPB flight. Several of these events have been detected and as their duration is in the order of only 1-2 GTUs, they are presumably CRs directly hitting the detector. (Image: Battisti et al., 2018)

Therefore, the laser generated events from the CLF which were recorded during the field tests (see Section 4.3) were used. An example how such an event looks like can be found in Section 4.3 and Fig. 4.3. The mean of the distribution of 270 reconstructed events was found to be at $(97.62 \pm 1.05)^\circ$, which perfectly matches the expectation of 97.8° as the instrument was tilted by 7.8° (Eser, 2018). The higher angular resolution achieved – compared to the result from EUSO-Balloon – is mainly because the exact position of the light source is known (Bertaina, 2019).

As already mentioned in Section 6.6, the results presented in this section are either results of the entire EUSO-SPB collaboration or performed by various members of the collaboration and are not part of this work. Thus, further details are not given and can be found for example in Bertaina, 2019 and Battisti et al., 2018. For a large amount of the data, the analyses are also still ongoing.

7 Summary and Conclusion

In the context of the research work reported in this thesis, I have conducted experimental studies essential for the development of a space-based telescope for the observation of UHECRs. Since no space-based UHECR missions have flown up to now, these studies are unprecedented, and conceptually innovative. More specifically, I have developed two key components of the digital electronics of the telescope, the Cluster Control Board (CCB) and the Photo-Detector Module (PDM) control board. Beside other functionalities, the CCB manages and combines data from a cluster of 8-9 PDMs, performs the second level trigger, and transfers the data to the Data Processor (DP). The PDM control board mainly interfaces the read-out electronics and performs the first level trigger. The digital electronics is therefore not a service module but, on the contrary, one of the key hardware elements of the mission, since it enables the core functionalities of the instrument. This includes the rather demanding first and second level trigger, and the transfer of scientific and ancillary data.

The work covered the full development of the electronic elements, from the definition of the requirements to the development and testing of prototypes, with the final goal of demonstrating the functional and technological readiness of these components. In the framework of the thesis, the developed components were integrated and tested in several pathfinder projects, realized by the JEM-EUSO collaboration in order to test the observation principle and the technological readiness of the various subsystems and of the integrated instrument elements. The pathfinders projects are:

- EUSO-TA, which is a ground based instrument operated in the desert of Utah at the Telescope-Array (TA) site.
- EUSO-Balloon, which was brought to near space on board of a stratospheric balloon in order to measure the fluorescence background component. In addition, it successfully recorded artificial EAS signatures which were generated by a laser on board of a helicopter flying through the FoV of the instrument.
- EUSO-SPB, which was operating for 12 days on board of a super-pressure balloon and successfully demonstrated the self triggering capabilities of the detector electronics and its autonomous operation.

As the first step of the developments presented here, and in the more general framework of the JEM-EUSO Phase-A study, the requirements for the electronics were defined. Based on these requirements, a prototype CCB for the JEM-EUSO mission was developed and several advanced options have been studied. The most demanding requirements imposed on the electronics are derived from the extremely low flux of the UHECR and the evolution of the EAS at nearly the speed of light, resulting in fast signals to be recorded. In addition, the solutions to be implemented had to meet the rather constraining requirements for their operation in space with limited resources and in a challenging radiation environment.

While actual space qualified hardware was not implemented (as it was not a requirement for the Phase-A study and due to cost considerations), all parts were carefully selected such that the key parameters of the commercial equivalent accurately resemble those of the available space qualified counterpart. Therefore, it was demonstrated that the technology is ready for the JEM-EUSO mission and that the board is able to interface and process up to nine PDMs, which exceeds the baseline requirement for JEM-EUSO. A study on new technology becoming available in radiation hard components showed that the performance of the integrated PPC405 processor cores or the DDR-SDRAM is sufficient to be considered as advanced options.

Based on the developments and studies done for the JEM-EUSO CCB, a smaller version of the CCB was developed for the pathfinder projects EUSO-TA, EUSO-Balloon, and EUSO-SPB, which demonstrated the soundness of the observation principle and the adequateness of the chosen technology. We also performed tests which are typically mandatory for space operations. With the carefully designed thermal structure of the CCB, it was possible to qualify the CCB for the required operational temperature range of the instrument radiator. During the thermal vacuum tests and the balloon flight operations, it was shown that the requirement on the operational temperature range could be exceeded by 40 % for the hot case, while the cold case requirement could be exceeded by at least 100 %. During the near-space balloon flights, the CCB proved to be robust and very reliable. It successfully performed all tasks related to the interfaces with the PDM and the DP, as well as the transfer of configuration, scientific and ancillary data from the DP towards the PDM and vice versa. The L2 trigger algorithm was successfully implemented and tested, but was not used during the EUSO-Balloon flight, because the L1 trigger algorithm (onto which the L2 trigger algorithm depends and which was still developed at the University of Torino/INFN Torino and at the University Paris Diderot/CNRS at this point of time) was not available in the PDM control board, as it did not fulfill the resource constraints of the implemented FPGA. During the EUSO-SPB flight, the L2 trigger algorithm was also not tested on board, because the L1 trigger algorithm proved to be sufficient to keep the trigger rate low – especially as the instrument consisted only out of one PDM.

For the EUSO-SPB flight, I re-designed the PDM control board and re-wrote and optimized the firmware of the FPGA. By implementing a new power distribution system, together with the revision of the electrical architecture of the instrument, the overall electrical noise was reduced and the reliability of the instrument was largely improved. In fact with the new implementation, several problems which emerged during the development of the PDM control board for EUSO-Balloon were solved. Based on the experience on the thermal structure of the CCB, I designed a similar system for the PDM control board. During thermal vacuum tests, the PDM control board was successfully operated between $-30\,^{\circ}\mathrm{C}$ to $+60\,^{\circ}\mathrm{C}$ without any problems, thus meeting and actually exceeding the requirements. Due to the performed optimization of the VHDL code, the L1 trigger algorithm was successfully implemented for all nine ECs and proved its capabilities to suppress spurious triggers to a level which complies with the downlink telemetry bandwidth. In particular, it was possible to keep the trigger rate below 2 Hz for the complete PDM during the EUSO-SPB flight.

In addition, the HV switching algorithm was implemented and an end-to-end test was performed. This test successfully demonstrated that the algorithm and the related periphery are able to increase the voltage of the photocathode, which results in a lower efficiency and thus in a reduction of the amount of photoelectrons reaching the first dynode of the MAPMT. As it was demonstrated that this happens within a few GTUs, the HV switching algorithm was used during the field-tests and during the EUSO-SPB flight to protect the MAPMTs in case of strong light conditions like thunderstorms.

In the framework of the thesis, all developed components and their functionalities were thoroughly tested. This started with the verification of the manufacturing process. During single component tests in laboratory environments, all functionalities were verified, which also included the verification of the performance requirements. During this first step, the priority was given to the data bandwidth of the external memories, the performance of the electrical interfaces towards other components, and the data processing capabilities of the trigger algorithms.

During the following instrument integrations and the field tests, the global interaction of the CCB and the PDM control board with other modules of the instrument was validated. The development, verification, and validation process finally culminated in the successful EUSO-Balloon and EUSO-SPB flights, which eventually proved that both boards were fully functional and fulfilled or even exceeded all requirements.

The successful development of the hardware and the implementation of the trigger algorithms enables UHECR observations from space and provides technology suitable for any such future mission devoted to the detection of UHECRs from space. Such a space-based mission will open a new scientific window: astronomy through the particle channel.

Acknowledgments

A scientific experiment is never the work of a single person. This is especially true for large and complex experiments such as JEM-EUSO. As part of an international collaboration, I have spend a lot of my time abroad working intensively with people originating literally from all-over the world. Consequently, the invaluable experiences I gained during that time are not limited to 'technical know-how'. I really enjoyed the time I had at the institute, the time during the sometimes quite stressful integration campaigns and of course the exciting balloon flight campaigns – it was a great experience for me. Therefore, I would like to express my gratitude to all the people who supported me during the time of the thesis and my studies. Especially, I am pleased to thank the following people:

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List of Acronyms

ADC	Analog-to-Digital-Converter
AGM	Absorbent Glass Mat
AMS	Atmospheric Monitoring System
ASIC	Application Specific Integrated Circuit
BGA	Ball Grid Array
BPI	Byte-wide Peripheral Interface
BRAM	Block Random-Access Memory
CCB	Cluster Control Board
CLB	Configurable Logic Block
CLF	Central Laser Facility
CLKB	Clock Board
CMBR	Cosmic Microwave Background Radiation
CNES	Centre National d'Études Spatiales
CNRS	Centre national de la recherche scientifique
COSI	Compton Spectrometer and Imager
COTS	Commercial Off-The-Shelf
CPU	Central Processing Unit
CR	Cosmic Ray
CRC	Cyclic Redundancy Check
CSA	Canadian Space Agency
CSBF	Columbia Scientific Balloon Facility
DC	Direct Current
DC/DC	Direct Current to Direct Current
DDR	Double Data Rate
DDR-SDRAM	Double Data Rate-Synchronous Dynamic Random-Access Memory
DIP	Dual In-line Package
DMA	Direct Memory Access
DP	Data Processor
DRAM	Dynamic Random-Access Memory
DSP	Digital Signal Processor
EAS	Extensive Air Shower
EC	Elementary Cell
ECC	Error Correcting Code
EMAC	Ethernet Media Access Controller

ESA	European Space Agency
ESAF	EUSO Simulation and Analysis Framework
EUSO	Extreme Universe Space Observatory
EUSO-Balloon	Extreme Universe Space Observatory-Balloon
EUSO-SPB	Extreme Universe Space Observatory-Super-Pressure Balloon
EUSO-TA	Extreme Universe Space Observatory-Telescope-Array
FEE	Front-End Electronics
FF	Flip-Flop
FIFO	First In First Out
FoV	Field-of-View
FPGA	Field Programmable Gate Array
FS	Focal Surface
GLS	Ground Laser System
GMII	Gigabit Media Independent Interface
GPIO	General-Purpose Input/Output
GPS	Global Positioning System
GSE	Ground Support Equipment
GTU	Gate Time Unit
GZK	Greisen-Zatsepin-Kuzmin
HDL	Hardware Description Language
HK	Housekeeping
HTV	H-II Transfer Vehicle
HV	High Voltage
HVPS	High-Voltage Power Supply
I/O	Input/Output
IC	Integrated Circuit
ICDV	Instrumentation Chaîne De Vol
INFN	Istituto Nazionale di Fisica Nucleare
INTC	INTerrupt Controller
IR	InfraRed
ISS	International Space Station
JACEE	Japanese-American Cooperative Emulsion Experiment
JAXA	Japan Aerospace Exploration Agency
JEM-EUSO	Extreme Universe Space Observatory on board the Japanese Experiment Module
JEM	Japanese Experiment Module
L1	Level 1
LED	Light-Emitting Diode
LIDAR	LIght Detection And Ranging
LTT	Linear Track Trigger
LUT	Look Up Table

LVDS	Low-Voltage Differential Signaling
LVPS	Low-Voltage Power Supply
lwIP	LightWeight Internet Protocol
MAPMT	Multi Anode PhotoMultiplier Tube
MCU	MicroController Unit
MDP	Mission Data Processor
MGT	Multi-GigaBit Transceiver
MUX	Multiplexer
NASA	National Aeronautics and Space Administration
NEV	Nacelle EnVeloppe
NIST	National Institute of Standards and Technology
NOR	Not OR
NOSYCA	NOuveau SYstème de Contrôle d'Aérostats
NRTA	Near Real Time Analysis
NSO	Nacelle de Servitude Opérationnelle
OM	Optics Module
PAO	Pierre Auger Observatory
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect
PDM	Photo-Detector Module
PDN	Power Distribution Network
PHY	Physical Layer
PLB	Processor Local Bus
PLL	Phase-Locked Loop
PMMA	PolyMethylMethAcrylate
PPC405	PowerPC 405
PPS	Pulse Per Second
PROM	Programmable Read-Only Memory
PSF	Point Spread Function
PTT	Persistency Tracking Trigger
PWP	PoWer Pack
QFN	Quad-Flat No-leads
RAM	Random-Access Memory
RC	Resistor-Capacitor
RMS	Root Mean Square
ROM	Read-Only Memory
RUNJOB	RUssia Nippon JOint Balloon
SD	Secure Digital
SDRAM	Synchronous Dynamic Random-Access Memory
SiECA	Silicon photomultiplier Elementary Cell Addon
SIMEON	SIMulateur Environnement Opérationnel Nacelles

SIP	Support Instrumentation Package
SiPM	Silicon PhotoMultiplier
SIREN	Système d'Interface REseau NOSYCA
SPACIROC	Spatial Photomultiplier Array Counting and Integrating Read-Out Chip
SPB	Super-Pressure Balloon
SPDT	Single Pole Double Throw
SPI	Serial Peripheral Interface
SRAM	Static Random-Access Memory
SSD	Solid State Drive
SSTL	Stub Series Terminated Logic
SuperTIGER	Super Trans-Iron Galactic Element Recorder
TA	Telescope-Array
TBC	To Be Confirmed
TBD	To Be Defined
TDRSS	Tracking Data Relay Satellite System
TID	Total Ionizing Dose
TLE	Transient Luminous Event
ToI	Time interval Of Interest
TRL	Technology Readiness Level
UART	Universal Asynchronous Receiver Transmitter
UCIRC	University of Chicago Infrared Camera
UHECR	Ultra-High-Energy Cosmic Ray
USB	Universal Serial Bus
UTC	Coordinated Universal Time
UV	UltraViolet
VHDL	Very high-speed integrated circuit Hardware Description Language
XPE	XPower Estimator