Single Electron Transistors in CMOS Compatible Silicon MOSFETs

Dissertation
der Mathematisch-Naturwissenschaftlichen Fakultät
der Eberhard Karls Universität Tübingen
zur Erlangung des Grades eines
Doktors der Naturwissenschaften
(Dr. rer. nat.)

vorgelegt von
Dharmraj Kotekar-Patil
aus Hubli Dharwad, Karnatak, Indien

Tübingen
2012

Tag der mündlichen Prüfung: 19.02.2013
Dekan: Prof. Dr. Wolfgang Rosenstiel
1. Berichterstatter: Prof. Dr. Dieter P. Kern
2. Berichterstatter: Prof. Dr. David Wharam

Abstract

In this thesis conductance measurements are presented on electron transport through quantum dots. The devices are fabricated on a large scale with standard CMOS technology processes. Conductance measurements are performed initially at room temperature. Then the device is cooled down to $4.2K$ in a helium dewar and if necessary cooled down in a dilution refrigerator to the sub-$100mK$ temperature range.

Conductance measurements on a device with a single island showed clear Coulomb oscillations in the linear regime and Coulomb diamonds in the non-linear regime at $4.2K$. Conductance measurements in the linear regime on a device with relatively large dimensions showed metallic properties with equally spaced Coulomb oscillations, whereas conductance measurements in the linear regime on a device with small dimensions showed aperiodic Coulomb oscillations, which are essentially a feature of a quantum dot. In the non-linear regime, devices with small dimensions showed clear excited states. Charging energy as high as $40meV$ was observed.

Electron transport through a double dot in series is studied at $4.2K$. By tuning the gate voltage, the strength of coupling between the two dots can be tuned. Conductance measurements in the linear regime on such a device clearly showed a transition from weakly tunnel coupled dots to a strongly tunnel coupled dot. From the conductance measurement it was possible to extract capacitive parameters, which are used in a simulation which agrees with the measurements. Taking advantage of advanced fabrication technology, devices with triple quantum dots in series were fabricated in the framework of a EU project. These devices are compact such that three quantum dots are tuned using just two gates. Simulations are performed based on an electrostatic model which agrees very well with the measured data. Conductance measurements on more complex designs with a single top gate and two side gates gave an additional degree of freedom.

Upon cooling down the devices below a certain temperature, charging effects in the gate are seen. These charging effects are due to individual grains in the polysilicon gate acting as a quantum dot and the grain boundaries as tunnel barriers. If the temperature of the system is sufficiently low so that the charging energy of the grain in the polysilicon gate is larger than the thermal energy, then the transport of electrons in the polysilicon grain is dominated by Coulomb charging. These charging events in the polysilicon gate gave rise to novel features in the conductance measurements. An electrostatic model is presented which explains the origin of these novel features very well.

Abstract

In dieser Arbeit werden Leitwertsmessungen zum Elektronentransport durch Quantenpunkte vorgestellt. Die Bauelemente werden großflächig mit Standard-CMOS-Technologie hergestellt. Leitwertsmessungen werden zunächst bei Raumtemperatur durchgeführt. Dann wird das Element in einem Helium-Dewarbehälter auf $4,2K$ abgekühlt oder wenn nötig in einem Entmischungskryostat auf Temperaturen unter $100mK$ gekühlt.

Leitwertsmessungen bei $4,2K$ an einem Element mit einer einzelnen Insel zeigen klare Coulomb-Oszillationen im linearen Transportregime und Coulomb-Diamanten im nichtlinearen Transportregime. Leitwertsmessungen im linearen Transportregime an einem Element mit relativ großen Abmessungen weisen eine metallische Charakteristik mit Coulomb-Oszillationen in regelmäßigen Abständen auf, wohingegen lineare Transportmessungen an einem Element mit kleinen Abmessungen aperiodische Coulomb-Oszillationen zeigen, die ein charakteristisches Kennzeichen eines Quantenpunkts sind. Im nichtlinearen Transportregime wiesen Elemente mit kleinen Dimensionen klare Anregungszustände auf. Es wurden Ladeenergien bis zu $40meV$ beobachtet.

Elektronentransport durch einen seriellen Doppel-Quantenpunkt wurde ebenfalls bei $4,2K$ untersucht. Indem die Gatespannung variiert wird, kann die Kopplungsstärke zwischen den beiden Quantenpunkten eingestellt werden. Lineare Leitwertsmessungen an einer solchen Probe zeigen deutlich einen Übergang von schwach tunnelgekoppelten Quantenpunkten zu einem stark tunnelgekoppelten Quantenpunkt. Aus den Leitwertsmessungen konnten die Kopplungskapazitäten extrahiert werden, die als Parameter in eine Simulation eingesetzt wurden, die gute Übereinstimmung mit den Messungen zeigt. Mit Hilfe von hochentwickelter Herstellungstechnologie wurden im Rahmen eines EU-Projekts Elemente mit seriellen Dreifach-Quantenpunkten hergestellt. Diese Elemente sind sehr kompakt, so dass die drei Quantenpunkte mit nur zwei Gate-Elektroden gesteuert werden können. Mit einem elektrostatischen Modell wurden Simulationen durchgeführt, die sehr gut mit den gemessenen Daten übereinstimmen. Leitwertsmessungen an komplexeren Designs mit einer einzelnen Top-Elektrode und zwei seitlichen Elektroden boten einen weiteren Freiheitsgrad.

Sobald die Elemente unter eine bestimmte Temperatur abgekühlt werden, werden Ladeeffekte in der Gate-Elektrode sichtbar. Die Ursache dieser Ladeeffekte ist, dass einzelne Körner der Polysilizium-Elektrode sich wie ein Quantenpunkt verhalten, wobei die Korngrenzen Tunnelbarrieren bilden. Wenn die Temperatur des Systems ausreichend niedrig ist, damit die Ladeenergie des Korns in der Polysilizium-Elektrode gegenüber der thermischen Energie überwiegt, wird der Elektronentransport durch das Polysilizium-Korn durch Coulomb-Ladeeffekte dominiert. Diese Ladeeffekte in der Polysilizium-Elektrode führten zur Beobachtung neuer Effekte in den Leitwertsmessungen. Das hier präsentierte elektrostatische Modell kann den Ursprung dieser neuartigen Effekte sehr gut erklären.

Contents

Chapter 1

Introduction

1.1 Context

After the invention of the first bipolar transistor in 1947, there has been rapid progress in the semiconductor industry. The bipolar transistor was replaced by the Field Effect Transistor (FET) in the 1960s and FETs were soon used in logic circuits. Since then, the size of the logic devices has been decreasing, particularly the gate length. The aim of the semiconductor industry was to make the transistor smaller for three reasons:

1. Faster switching time
2. Increasing the density of devices in a given area which would reduce the cost and provide more functionality
3. Reducing the power consumption

In 1965, Gordon Moore stated an empirical law which says that the number of transistors in a given area doubles every 18 months [known as "Moore's law"]. Moore's law has allowed the semiconductor industry to synchronize development in device fabrication and architechture. Since then, the semiconductor industry has been trying to keep pace with predictions made by Moore's law and this has been institutionalized with the International Technology Roadmap for Semiconductors (ITRS) [1]. Fig. 1.1 shows Moore's law.

Silicon is one of the most studied materials and has been the material of choice for microelectronics over the past years. This has led to the achievement of a high level of perfection in silicon technology, in particular, the interface between silicon and the silicon dioxide (gate oxide) is essentially free of defects. The progress of silicon Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) will continue for the next few years, according to the ITRS. But the shrinking dimensions have led to several problems where quantum mechanical effects such as tunneling and short channel effects are degrading the performance of the transistors. With the shrinking gate length, the ON/OFF ratio of the source-drain current is decreasing and hence, efforts are being made to improve the gate control using high dielectrics and several gate electrodes.

Another advantage of Si-MOSFETs is that the fabrication process is well established and so it would be convenient to continue with this technology. But as the dimensions get smaller, the devices suffers from several problems such as:

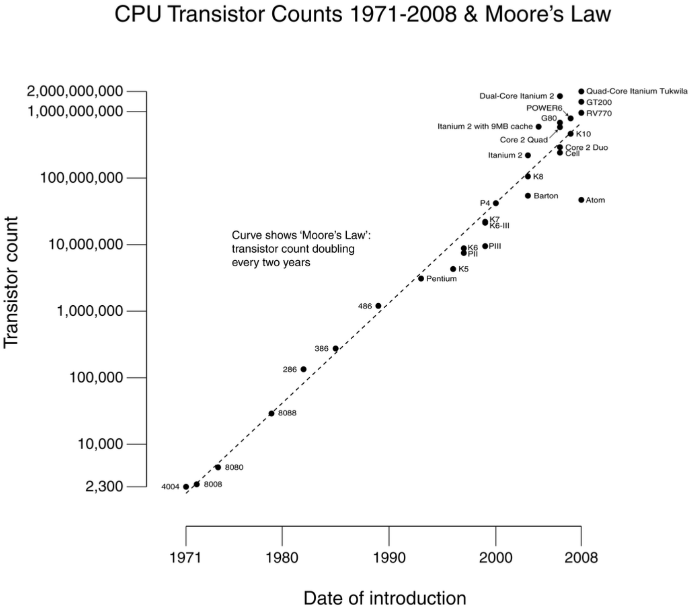

Figure 1.1: Moore's law showing the number of transistors doubling every two years [1].

1. For $10\,nm$ gate lengths, the electrostatic control of the gate over the channel becomes weaker. This leads to poor ON/OFF ratio of the source-drain current in the MOSFETs.
2. Short channel effects which results from decreasing the channel length. In the short channel MOSFETs, the potential barrier between the source and the drain is controlled by the gate voltage as well as the drain voltage (source grounded). If the drain voltage is increased, the potential barrier between the channel decreases and eventually current starts to flow between the source and drain even if the gate voltage is less than the threshold voltage. This current flowing between the source-drain below the threshold voltage is called sub-threshold current.
3. Thinner gate oxides between the gate and the channel lead to current flow between the gate and the channel (gate leakage current) on application of gate voltage. This is an undesired effect.

The solution to a weaker gate effect is a double gate, which provides better electrostatics than a single gate. The short channel effects can be improved by changing the doping profile in the channel, source and the drain which allows change in the distribution of the electric fields and the potential profile between the source, drain and the channel. The doping profiles can be optimized to minimize the sub-threshold current and maximize the ON current. The solution to thinner gate oxide, which results in gate leakage could be the use of high dielectric material. This would eliminate the gate leakage problem.

An alternate solution to MOSFETs is the Single Electron Transistor (SET). It will be suitable to be implemented in the industry if it satisfies the following two conditions:

1. It should be compatible with standard Complementary Metal Oxide Semiconductor (CMOS) technology

2. It should work at room temperature

There are several advantages and applications of the SET over the bulky MOSFET. The MOSFET is turned ON once and the current is measured in microamperes whereas the SET is turned ON every time an electron flows through the device. The power consumption is roughly proportional to the number of electrons transferred from the voltage source to the ground. This reduces the power consumption and makes the SET a good candidate for use in Ultra Large Scale Integration (ULSI). The SET can be used as a charge sensor (electrometer). The current in the SET is extremely sensitive to the variation of charge in the vicinity. A small change in the charge leads to a measureable variation in the current through the SET. Another application of the SET is a radio frequency turnstile device. By turning the barriers ON and OFF sequentially one can generate a current $I = ef$ (where e is the electron charge and f is the radio frequency)[2][3]. The SET in an undoped silicon nanowire can act as a quantum dot [4]. The discrete density of states in the semiconductor quantum dot makes it is possible to observe the first electrons on the dots. With smaller quantum dots where the single particle level spacing is higher than the thermal energy $k_B T$, it is possible to observe individual quantum mechanical states. Two SETs placed in series can form a coupled dot system forming a two level system which can be used as a qubit. Also, the spin of dopant states in silicon can have very long relaxation times because of the very weak spin–orbit interaction and because the isotope $^{14}_{28}Si$ has a nuclear spin 0 [5][6].

The work done in this thesis stands at the interface of technology and physics. From the physics point of view, we try to study the atomic properties of the quantum dots i.e. level spectroscopy, etc, whereas the from technology point of view, we try to study the key issues of variability and reproducibility in the devices. The devices are fabricated on a large scale on standard CMOS technology. The work in this thesis is done under the Atomic Functionalities on Silicon Devices (AFSID) project sponsored by the European Union (EU) [7].

1.2 Outline of the Thesis

In this thesis we present measurements on the SETs with a simple geometry having a single gate to a more complex one with multigate devices. In a very simple geometry device having a single top gate, the quantum dot in the device is defined by the gate electrode which covers the central part of the channel. Such devices form the basis for more complex geomerty.

In chapter 2, we discuss the theory of the Coulomb blockade. We begin by discussing a classical electrostatic model with just three electrodes and calculate the current through the device using the master equation technique. We also treat metallic SETs and the quantum dot in two different sections in detail. The simulations performed in this work are based on the theory discussed in this chapter.

In chapter 3, we discuss briefly the fabrication process. Chapter 3 also discusses the process through which a device goes from the wafer level to the measurement set-up.

Chapter 3 also discusses the working of the dilution refrigerator which allow us to cool down the devices to sub-100mK regime. Cooling the devices to such a low temperature reduces the level of noise, hence improving the signal-to-noise ratio and the clarity of the measured data. Finally, chapter 3 discusses the experimental set-up used to perform the measurements.

The characterization of the devices are presented in chapter 4. The characterization starts initially with room temperature measurement. Later, the devices are cooled down to $4.2K$ in a helium bath. If necessary, devices are also cooled down in a dilution refrigerator to sub-100mK regime. We discuss how the devices working as a MOSFET at room temperature become a single electron transistor at low temperature. We demonstrate the SET operation in a metallic regime as well as in a quantum dot regime. The effect of asymmetric tunnel barriers is shown using simulations and confirmed in measurements. We also discuss the theory of the double dot system and present measurements on such a system. Furthermore, we present measurements on triple quantum dots in series where simulations have been done to explain the details observed in the measurements. Using a more complex device geometry, we also show the effect of unintentionally formed quantum dots on the transport properties.

In chapter 5, we discuss the formation of grain boundaries in polysilicon. At low temperatures, we observe charging effects in the polysilicon grains, which produce novel features in the measurements in the non-linear regime. We explain these features by giving an electrostatic model and perform simulations which match the measurements very well. These charging effects are also studied in complex geometry devices in the linear regime.

Chapter 2

Theory of Coulomb blockade

2.1 Introduction

If an island is weakly tunnel coupled to metallic leads, then for a small bias voltage the current through the device is suppressed (highly resistive). If an sufficiently large bias voltage is applied, the current begins to flow through the device. This suppression of the current at small bias voltages is known as the Coulomb blockade. The Coulomb blockade phenomenon occurs because the electrons already existing on the island try to repel the electrons coming from the metallic leads. This results in suppression of the current at small bias votlages. In order to overcome this repulsion, sufficiently high bias voltage must be applied. Fig. 2.1 exhibits the phenomenon of Coulomb blockade at $T = 0K$. At bias voltage less than $\pm V_B$ the current through the device is completely suppressed whereas the current increases with increase in bias voltage for voltages greater than $\pm V_B$. Coulomb blockade was first studied in the system with a metallic island separated from metal leads (source and drain) by tunnel barriers [8][9][10]. Barriers can be of any type, provided they have sufficiently high resistance $(R_t \gg \frac{h}{e^2})$ where R_t is the barrier resistance, e is the electron charge and h is the Planck's constant.

In a system with a single island, the island is separated from the source and the drain by tunnel barriers and hence, the electronic charge on the dot is quantized [11]. Each time a tunneling event occurs, i.e. an electron jumps from the source to the island or moves from the island to the drain electrode, the charge on the island fluctuates by an amount e. Such a change is associated with the charging energy $\frac{e^2}{C_\Sigma} = eV_B$, where C_Σ is the total capacitance of the island ($C_\Sigma = C_g + C_S + C_D$ where C_g, C_S and C_D are the gate, the source and the drain capacitance respectively) and V_B is the potential required to overcome the Coulomb blockade. When an electron jumps on the island, its electrostatic energy is increased by the amount $\frac{e^2}{C_\Sigma}$. The condition to see a Coulomb charging effect [12] is that the charging energy $\left(\frac{e^2}{C_\Sigma}\right)$ must be greater than the thermal energy $k_B T$. If the reverse is true i.e. $k_B T > \frac{e^2}{C_\Sigma}$, then the number of electrons on the dot is not quantized and hence, no charging effects can be seen.

A second requirement for the observation of single electron phenomena is that the wave function of electrons on the island must be localized; in other words, the tunnel barriers must be sufficiently opaque, so that quantum fluctuations of the number of electrons on the island (n) are negligible on the time scale of the measurements. This condition can

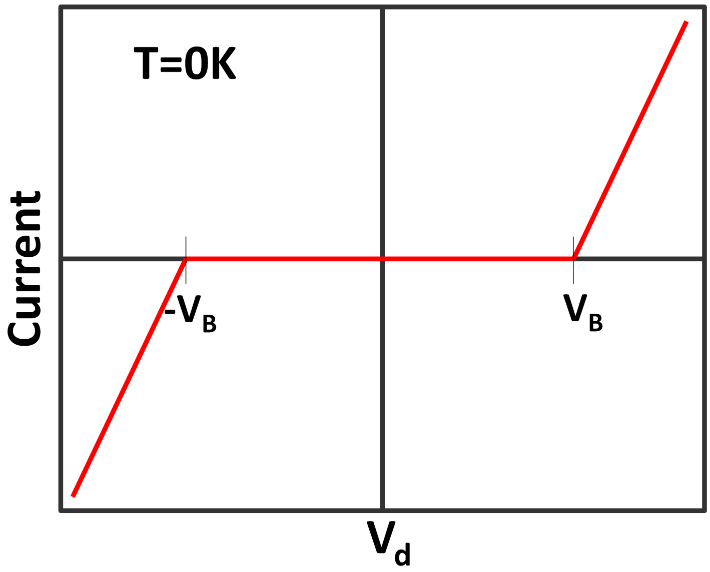

Figure 2.1: Current as a function of the bias voltage at $T = 0K$.

be expressed quantitatively considering the Heisenberg uncertainty relation $\Delta E \Delta t \geq h$. The energy scale of the Coulomb charging effect is given by the charging energy $\frac{e^2}{C_\Sigma}$ and its time scale by $R_t C_\Sigma$. Using the charging energy $\frac{e^2}{C_\Sigma}$ for energy and the time scale $R_t C_\Sigma$ for time in the Heisenberg uncertainty relation, this yields the following condition for R_t: $R_t \gg \frac{h}{e^2}$, where $\frac{h}{e^2} = 25.813k\Omega$ is the fundamental quantum of resistance.

To summarize the conditions for the Coulomb charging [12]:

$$R_t \gg \frac{h}{e^2}$$

$$\frac{e^2}{C_\Sigma} \gg k_B T$$

The first condition is satisfied by coupling an island weakly to the source and the drain via tunnel barriers. The tunnel barriers should be transparent enough to allow the electrons to pass through the barriers if sufficient energy is supplied to them. At the same time, the barriers should be opaque enough to maintain quantized electron number on the island if the electrons coming from the leads have energy less than the electrostatic charging energy. The second condition puts another restriction on the dimension of the device. The total capacitance of the dot must be small enough so that the charging energy is greater than the thermal energy. The dot with a total capacitance smaller than $4.4 \cdot 10^{-16}F$ is needed to see the charging effect because charging energy corresponding to capacitance $4.4 \cdot 10^{-16}F$ is approximately $0.36meV$ which is the thermal energy available at the liquid helium temperature $(4.2K)$.

2.2 Single Electron Box

In this section we consider the Coulomb charging effects in the Single Electron Box (SEB) following the theoretical description considered in ref. [13]. SEB is the simplest circuit which exhibits Coulomb charging effect [14][15]. The SEB is a simple circuit which consists of a tunnel junction and a storage capacitor. The tunnel junction is modelled as a capacitor of capacitance C_1 and a resistor of resistance R_1 in parallel. The storage capacitor C_b is a purely capacitive element which allows charge to accumulate on the capacitor C_b and does not allow charge to flow through it. The island lies between these two capacitors C_1 and C_b. A bias voltage is used to transfer electrons across the tunnel junction C_1, onto or off island. The resistance R_1 of the tunnel junction allows electron transfer between the island and the voltage supply whereas C_1 allows the charge Q_1 to accumulate across the tunnel junction C_1. The charge Q_1 on the tunnel junction is a continuous variable.The change in the charge Q_1 can be fractionally small since it depends on the displacement of the electrons in the electrodes relative to their ionic background. The storage capacitor C_b isolates the island charge from its environment and makes it possible to observe Coulomb blockade even in a low impedence environment. The two capacitors, C_b and C_1, of the SEB are in series and hence the equivalent capacitance is given by:

$$C_{eq} = \frac{C_1 C_b}{(C_1 + C_b)} \tag{2.1}$$

with a charge

$$Q_{eq} = \frac{(Q_1 C_b + Q_b C_1)}{(C_1 + C_b)} \tag{2.2}$$

where Q_1 and Q_b are charges on C_1 and C_b respectively. Charge on the island is $-ne = Q_1 - Q_b$ and only the Q_{eq} is affected by the environment. This allows us to observe Coulomb blockade in a low impedance environment as well. If the bias voltage V is increased, charge Q_1 accumulates on the capacitor C_1 resulting in tunnel junction voltage V_1 across C_1. Similarly, with increase in the bias voltage, charge Q_b accumulates on the capacitor C_b resulting in voltage V_b across C_b. We recall that the electrons can tunnel onto or off the island via the tunnel junction C_1. The charge across C_1 increases until it exceeds the critical charge value [3][16][17][18]

$$Q_c = \frac{eC_1}{2(C_1 + C_b)} \tag{2.3}$$

and the Coulomb blockade is overcome. The charge on the island changes from Q_1 to $Q_1 - e$ which is less than Q_c. The Coulomb blockade is then reimposed and the electron is trapped on the island. By further increasing V, the Coulomb blockade can be overcome periodically and trapping additional electrons on the island.

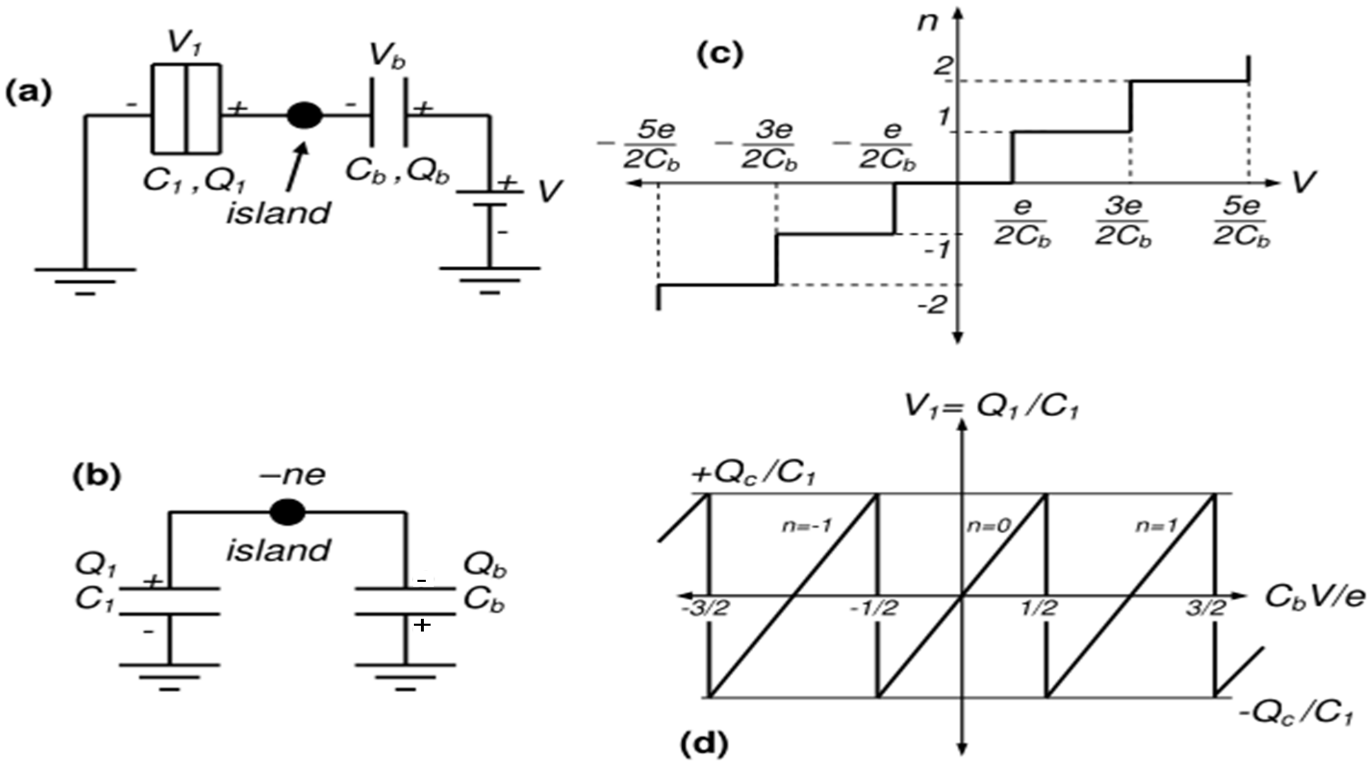

Figure 2.2: a) Circuit diagram of the SEB. The circuit shows charge built-up on the tunnel junction and on the storage capacitor. b) Equivalent circuit of a) looking from the island. c) Plot of the island charge as a function of the supply voltage V. d) Voltage across the tunnel junction as a function of the bias voltage V. This figure is taken from ref. [13].

The electrostatic energy of the SEB for an electron added onto the island can be calculated by calculating the charge Q_1 and Q_b on the capacitors C_1 and C_b respectively. When an electron is added to the island it creates a non-equilibrium condition, and the equilibrium condition is re-established by charge transfer from the supply voltage V.

Fig. 2.2a shows the circuit diagram of a SEB. Looking from the island, C_1 and C_b are parallel to each other (Fig. 2.2b) and the island charge is given by :

$$-ne = Q_1 - Q_b \tag{2.4}$$

where n corresponds to the number of electrons on the island.

Applying Kirchhoff's voltage law to the circuit:

$$V_1 + V_b - V = 0 \tag{2.5}$$

$$\frac{Q_1}{C_1} + \frac{Q_b}{C_b} - V = 0 \tag{2.6}$$

Solving eq. 2.5 and eq. 2.6 simultaneously, Q_1 and Q_b can be found in terms of ne and V.

$$Q_1 = \frac{C_1}{C_\Sigma}(C_b V - ne) \tag{2.7}$$

$$Q_b = \frac{C_b}{C_\Sigma}(C_1 V + ne) \tag{2.8}$$

where $C_\Sigma = C_1 + C_b$ and is the total capacitance of the circuit.

If an electron tunnels onto the island across the tunnel capacitor C_1, the charge on the island changes from $-ne$ to $-ne - e$. This changes the tunnel junction charge Q_1 as follows:

$$\Delta Q_1 = Q_{1,final} - Q_{1,initial} = -\frac{C_1}{C_\Sigma}e \tag{2.9}$$

Similarly, the charge on the storage capacitor changes by:

$$\Delta Q_b = Q_{b,final} - Q_{b,initial} = \frac{C_b}{C_\Sigma}e \tag{2.10}$$

The above eq. 2.9 and eq. 2.10 imply that the island charge changes by $-e$, i.e. $\Delta Q_1 - \Delta Q_b = -e$ consistent with the eq. 2.4.

Knowing the change in the charge on each capacitor allows us to calculate the electrostatic energy of the circuit when an electron tunnels onto or off the island.

The total change in the electrostatic energy is given by the sum of changes in the charging energy of the island and the energy supplied by the voltage supply V:

$$\Delta E_\pm = E_{final} - E_{initial} + Energy\,supplied\,by\,the\,voltage\,sources$$

$$= \frac{(-(n \pm 1)e)^2}{2C_\Sigma} - \frac{(-ne)^2}{2C_\Sigma} \mp V\Delta Q_b \tag{2.11}$$

where E_{final} and $E_{initial}$ is the energy of the circuit after and before the electron transfer respectively. $\triangle E_\pm$ is the change in the electrostatic energy where $+$ and $-$ indicate the energy needed to add and remove an electron from the island respectively [19].

$$\Delta E_{\pm} = \frac{e}{C_{\Sigma}}\left(\mp C_b V \pm ne + \frac{e}{2}\right) \tag{2.12}$$

Eq. 2.12 can be used to calculate the tunneling rate for the electrons tunneling on or off the island.

We now calculate the tunneling rate through the tunnel barrier 1. The total Hamiltonian for the system is written as [3]:

$$H = H_{electrode} + H_{env} + H_{\Gamma}$$

where $H_{electrode}$ is the Hamiltonian for the electrode, H_{env} is the Hamiltonian describing the environment and H_{Γ} is the Hamiltonian describing the tunneling. If H_{Γ} is small enough, we can treat tunneling Hamiltonian as a perturbation and tunneling rate may be calculated using the golden rule approximation. We include the interaction term ΔE, which allows us to to relate the change in the energy ΔE due to the tunneling event with a tunnel rate $\Gamma(\Delta E)$. The tunneling rate using the golden rule approximation can be written as:

$$\Gamma_{i\rightarrow f} = \frac{2\pi}{\hbar}\,|< initial \mid H_{\Gamma} \mid final >|^2\, \delta(E_{initial} - E_{final} - \Delta E)$$

The above equation gives us the rate of transitions between the inital state $|initial>$ and the final state $|final>$. $< initial \mid H_{\Gamma} \mid final >$ describes the coupling between the left and the right hand side of the tunnel barrier. The dirac delta function ensures that the tunneling event takes place only if the initial state has the same energy as the sum of final state and change in energy when a tunneling event takes place.

$$\Gamma_{i\rightarrow f} = \frac{2\pi}{\hbar}\sum_i\sum_j |< initial \mid H_{\Gamma} \mid final >|^2 f(E_{initial})\left[1 - f(E_{final})\right] \delta(E_{initial} - E_{final} - \Delta E)$$

where $f(E)$ is the fermi-dirac distribution which gives the probability of an energy level being occupied whereas $1 - f(E)$ is the probability of an energy level being empty.

$$f(E) = \frac{1}{(1+\exp(\frac{E-E_F}{k_B T}))} \text{ and } 1 - f(E) = f(-E) = \frac{1}{(1+\exp(\frac{-E+E_F}{k_B T}))}$$

The term $|< initial \mid H_{\Gamma} \mid final >|$ is refered to as tunnel transmission coefficient, T and $|< initial \mid H_{\Gamma} \mid final >|^2$ is refered to as the transmission probability, $|T|^2$. For a small variation of tunnel transmission coefficient with energy, it is a reasonable approximation to treat the transmission probability as a constant and can be taken out of the summation.

$$\Gamma_{i\to f} = \frac{2\pi}{\hbar} \mid T \mid^2 \sum_i \sum_j f(E_{initial}) \left[1 - f(E_{final})\right] \delta(E_{initial} - E_{final} - \Delta E)$$

Since the electrode is metallic it consists of large number of states, we have to integrate over all energies for the states with non-zero tunneling probability. The density of states gives us the number of states in a small energy range dE and is given by $D(E)dE$. Density of states can be used to convert the sum over the energy into integral over all the states with non-zero tunneling probability.

$$\Gamma_{i\to f} = \frac{2\pi}{\hbar} \mid T \mid^2 \int_{E_{c,i}}^{\infty} dE_{initial} \int_{E_{c,f}}^{\infty} dE_{final} D_{initial}(E_{initial}) D_{final}(E_{final})$$

$$f(E_i) \left[1 - f(E_f)\right] \delta(E_{initial} - E_{final} - \Delta E)$$

where $E_{c,initial}$ is the conduction band edge where the electron resides initially whereas $E_{c,final}$ is the conduction band edge where the electron tunnel to in the final state. The main contribution of the integral in the above equation comes from the narrow window $f(E_i)\left[1 - f(E_f)\right]$ and the density of states is nearly constant near the fermi energy and it can be taken out of the integral. The delta function reduces one of the integrations such that

$$\Gamma_{i\to f} = \frac{2\pi}{\hbar} \mid T \mid^2 D_{initial} D_{final} \int_{E_c}^{\infty} dE f(E) \left[1 - f(E - \Delta E)\right]$$

using the relation:

$$\int_{-\infty}^{\infty} dE f(E) \left[1 - f(E - x)\right] = \frac{-x}{1 - e^{\beta x}}$$

we get

$$\Gamma = \frac{1}{e^2 R_1} \frac{-\Delta E_{\pm}}{1 - \exp\left(\frac{\Delta E_{\pm}}{k_B T}\right)} \tag{2.13}$$

where k_B is the Boltzmann constant and T is the electron temperature and R_1 is the resistance of the tunnel barrier given by:

$$R_1 = \frac{\hbar}{2\pi \mid T \mid^2 D_{initial} D_{final}}$$

At $T = 0K$ eq. 2.13 reduces to:

$$\Gamma = \frac{-\Delta E_\pm}{e^2 R_1} \ldots if \, \Delta E_\pm < 0$$

$$\Gamma = 0 \ldots if \, \Delta E_\pm > 0 \tag{2.14}$$

The tunnel resistance R_1 appears only in the eq. 2.13 and is significant in determining the tunnel rate for a transition in the number of electrons n. Eq. 2.13 and eq. 2.14 define the Coulomb blockade region at $T = 0K$. In the Coulomb blockade region, an electron cannot tunnel on the island since $\Delta E_\pm > 0$, i.e. sum of the final charging energy and the work done is greater than the initial charging energy which occurs when $C_b V < \left(n + \frac{1}{2}\right) e$ for ΔE_+ and $C_b V > \left(n - \frac{1}{2}\right) e$ for ΔE_-. This gives the range for Coulomb blockade at $T = 0K$:

$$\left(n - \frac{1}{2}\right) e < C_b V < \left(n + \frac{1}{2}\right) e \tag{2.15}$$

For a given number n, if V is changed such that the value of $C_b V$ moves outside the range given by eq. 2.15, then n re-adjusts to satisfy eq. 2.15. Within the range of eq. 2.15, n is constant. This is demonstrated in fig. 2.2c. Here it is important to notice that the period of the steps depends on C_b and is given by $\frac{e}{C_b}$, whereas C_1 enters the temperature condition $\frac{e^2}{2(C_1 + C_b)} > k_B T$.

At $T > 0K$, the tunneling event takes place even for $\Delta E_\pm > 0$, but only within the energy range of $k_B T$. Hence, in fig. 2.2c the steps develop rounded edges at finite temperatures. With an increase in temperature, the rounding of the steps increases and eventually develops into a straight line when $k_B T \gg \frac{e^2}{2(C_1 + C_b)}$.

Eq. 2.12 for ΔE_+ can be rearranged and written as:

$$\Delta E_+ = \frac{e}{C_1} \left(\frac{e C_1}{2 C_\Sigma} - \frac{C_1 \left(C_b V - ne\right)}{2 C_\Sigma} \right) = \frac{e}{C_1} \left(Q_c - Q_1\right) \tag{2.16}$$

where $Q_c = \frac{e C_1}{2 C_\Sigma}$ and $Q_1 = \frac{C_1 (C_b V - ne)}{2 C_\Sigma}$.

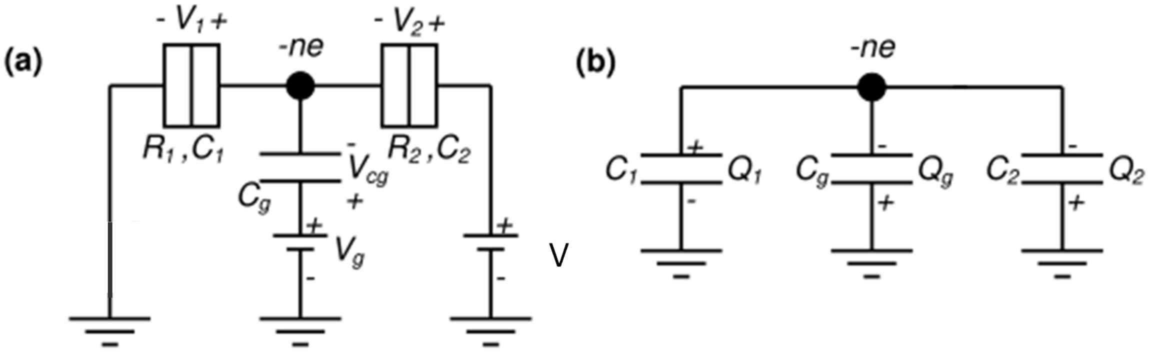

Figure 2.3: a) Circuit diagram of a SET. The circuit also shows the charge built-up on each tunnel junction C_1 and C_2 and the storage capacitor C_g. b) Equivalent circuit of a) looking from the island. This figure is taken from ref. [13].

From eq. 2.16, it can be seen that with an increase in V, the charge on the tunnel junction increases until it reaches Q_c and then an electron tunnels onto the island. Hence, the voltage across the tunnel junction V_1 varies between the limits $\pm\frac{Q_c}{C_1}$. If V increases, the voltage on the tunnel junction V_1 also increases until it reaches $\frac{Q_c}{C_1}$, then an electron tunnels onto the island. This changes the charge on the island from $(n \rightarrow n+1)$, and V_1 reduces to $-\frac{Q_c}{C_1}$ and the cycle of V_1 oscillating between $\pm\frac{Q_c}{C_1}$ continues. This is demonstrated in fig. 2.2d.

2.3 Single Electron Transistors

In this section, we follow the theoretical description in ref. [13]. A Single Electron Transistor (SET) is a device in which an island is tunnel-coupled to two electrodes, namely the source and the drain [20][21]. Each tunnel junction is represented as a capacitance and a resistance in parallel. We denote the capacitance of the left and the right tunnel junction as C_1 and C_2, whereas the resistances of the left and the right tunnel junction are denoted as R_1 and R_2 respectively. In the following circuit analysis, we assume a source electrode (tunnel junction 1) grounded and a drain electrode (tunnel junction 2) connected to the supply voltage. The island is also coupled to the third electrode called the gate. The gate is only capacitively coupled to the island via the capacitor C_g and no current flows between the gate and the island. The addition of this third gate electrode converts the double tunnel junction device into a SET (fig. 2.3a).

Using a similar analysis to the one in the last section, first the change in the electrostatic energy will be calculated when an electron tunnels onto or off the island across the two tunnel junctions, and then this change in electrostatic energy will be used to calculate the tunneling rate through each tunnel junction. Looking from the island (fig. 2.3b), C_1, C_2 and C_g are in parallel, and the charge $-ne$ on the island is given by [3]:

$$-ne = -Q_2 - Q_g + Q_1 \tag{2.17}$$

Applying Kirchhoff's voltage law to the left- and right-hand side loop in fig. 2.3a we obtain:

Left hand side loop (junction 1):

$$V_1 + V_{cg} - V_g = 0$$

$$\frac{Q_1}{C_1} + \frac{Q_g}{C_g} - V_g = 0 \tag{2.18}$$

Right hand side loop (junction 2):

$$V_g - V_{cg} + V_2 - V = 0$$

$$V_g - \frac{Q_g}{C_g} + \frac{Q_2}{C_2} - V = 0 \tag{2.19}$$

Solving eq. 2.17-2.19 simultaneously, we can find the charges Q_1, Q_2 and Q_g in terms of ne, V and V_g:

$$Q_1 = \frac{C_1}{C_\Sigma}\left(C_2 V + C_g V_g - ne\right) \tag{2.20}$$

$$Q_2 = \frac{C_2}{C_\Sigma}\left(\left(C_1 + C_g\right) V - C_g V_g + ne\right) \tag{2.21}$$

$$Q_g = \frac{C_g}{C_\Sigma}\left(-C_2 V + \left(C_1 + C_2\right) V_g + ne\right) \tag{2.22}$$

where $C_\Sigma = C_1 + C_2 + C_g$.

When the number of electrons on the island changes by one, the charge on each of the capacitors C_1, C_2 and C_g re-arranges itself in order to satisfy the condition given by eq. 2.17. Using eqs. 2.20-2.22, we can calculate the change in the charge on each capacitor. The change in the charge Q_1 on the tunnel junction C_1 is given by (using eq. 2.20):

$$\Delta Q_1 = Q_{1,final} - Q_{1,initial}$$

$$= \frac{C_1}{C_\Sigma}\left(C_2V + C_gV_g - (n+1)e\right) - \frac{C_1}{C_\Sigma}\left(C_2V + C_gV_g - ne\right)$$

$$\Delta Q_1 = -\frac{C_1}{C_\Sigma}e \tag{2.23}$$

and similarly, change in the charge Q_2 and Q_g can be calculated:

$$\Delta Q_2 = \frac{C_2}{C_\Sigma}e \tag{2.24}$$

and

$$\Delta Q_g = \frac{C_g}{C_\Sigma}e \tag{2.25}$$

Eq. 2.23, eq. 2.24 and eq. 2.25 imply that $-\Delta Q_2 - \Delta Q_g + \Delta Q_1 = -e$, i.e. island charge changes by $-e$. This is in agreement with eq. 2.17.

Knowing the change in the charge on each capacitor, the change in the electrostatic energy of the circuit can be calculated when an electron tunnels onto or off the island. This is given by change in the electrostatic energy of the island plus the energy supplied by the voltage sources when an electron tunnels on or off the island. For an electron tunneling onto the island across the tunnel junction C_1, the charge on each capacitor rearranges itself according to eq. 2.23-2.25, and the charge equilibrium is re-established by a transfer of charge through the voltage source. The work done by each voltage source is given by the magnitude of the voltage applied times the change in the charge on the associated capacitor given by eq. 2.23-2.25. The change in the electrostatic energy when an electron jumps onto the island through the tunnel junction 1 is given by [3][22]:

$$\Delta E_{1+} = E_{final} - E_{initial} + Energy\, supplied\, by\, the\, voltage\, sources$$

$$= \frac{\left(-(n+1)e\right)^2}{2C_\Sigma} - \frac{(-ne)^2}{2C_\Sigma} - V\Delta Q_2 - V_g\Delta Q_g$$

$$\Delta E_{1+} = \frac{e}{C_\Sigma}\left(ne + \frac{e}{2} - C_2V - C_gV_g\right) \tag{2.26}$$

A similar expression can be written for an electron tunneling off the tunnel junction C_1:

$$\Delta E_{1-} = \frac{e}{C_\Sigma}\left(-ne + \frac{e}{2} + C_2V + C_gV_g\right) \tag{2.27}$$

At $T = 0K$, eq. 2.26 and eq. 2.27 define the limits of the Coulomb blockade region for an electron tunneling across the first junction, as a function of V and V_g for n number of electrons on the island.

Similarly, the change in the electrostatic energy for an electron tunneling onto or off the second junction can be calculated as follows:

$$\Delta E_{2+} = \frac{e}{C_\Sigma}\left(ne + \frac{e}{2} + (C_1 + C_g)V - C_g V_g\right) \tag{2.28}$$

$$\Delta E_{2-} = \frac{e}{C_\Sigma}\left(-ne + \frac{e}{2} - (C_1 + C_g)V + C_g V_g\right) \tag{2.29}$$

Eq. 2.26,eq. 2.27,eq. 2.28 and eq. 2.29 can be used to calculate the tunneling rate across junctions 1 and 2. The tunneling rate can be calculated in the same way as shown for the case of SEB. The tunneling rate across tunnel junction 1 can be written as:

$$\Gamma_{1,\pm} = \frac{1}{e^2 R_1}\frac{-\Delta E_{1,\pm}}{1 - \exp\left(\frac{\Delta E_{1,\pm}}{k_B T}\right)} \tag{2.30}$$

where k_B is the Boltzmann constant, T is the electron temperature and R_1 is the resistance of the tunnel junction 1.

At $T = 0K$, eq. 2.30 can be written as:

$$\Gamma_{1,\pm} = \frac{-\Delta E_{1,\pm}}{e^2 R_1} \ldots if\, \Delta E_{1,\pm} < 0$$

$$\Gamma_{1,\pm} = 0 \ldots if\, \Delta E_{1,\pm} > 0 \tag{2.31}$$

A similar expression can be written for the tunneling rate across junction 2:

$$\Gamma_{2,\pm} = \frac{-\Delta E_{2,\pm}}{e^2 R_2} \ldots if\, \Delta E_{2,\pm} < 0$$

$$\Gamma_{2,\pm} = 0 \ldots if\, \Delta E_{2,\pm} > 0 \tag{2.32}$$

As in the case of the SEB, it is important to note that the tunnel resistances R_1 and R_2 appear only in eq. 2.31 and eq. 2.32 and are significant in determining the tunnel rate for a transition in the number of electrons n. In the Coulomb blockade region, an electron cannot tunnel onto or off the island since $\Delta E_{1,\pm} > 0$ for tunnel junction 1, i.e. the final charging energy and the work done is greater than the initial charging energy which occurs when $-C_2V - C_gV_g < \left(n + \frac{1}{2}\right) e$ for $\Delta E_{1,+}$ and $-C_2V - C_gV_g > \left(n - \frac{1}{2}\right) e$ for $\Delta E_{1,-}$. These expressions lead to the region of Coulomb blockade for $T = 0K$:

$$\left(n - \frac{1}{2}\right) e < -C_2V - C_gV_g < \left(n + \frac{1}{2}\right) e$$

and

$$\left(n - \frac{1}{2}\right) e < C_2V + C_gV_g < \left(n + \frac{1}{2}\right) e \tag{2.33}$$

Similarly, for tunnel junction 2, an electron cannot tunnel on or off the island for $\Delta E_{2,\pm} > 0$ and this leads to a region of Coulomb blockade for $T = 0K$:

$$\left(n - \frac{1}{2}\right) e < -C_1V + C_gV_g < \left(n + \frac{1}{2}\right) e$$

and

$$\left(n - \frac{1}{2}\right) e < C_1V - C_gV_g < \left(n + \frac{1}{2}\right) e \tag{2.34}$$

Within the Coulomb blockade region, the number of electron n trapped on the island is stable. For a given number of electron n, if V and V_g change such that it moves outside the range given by eq. 2.33 and eq. 2.34, then n re-adjusts itself so that the condition given by eq. 2.33 and eq. 2.34 is satisfied.

At $T > 0K$, the tunneling event takes place even for $\Delta E_{1\pm} > 0$ but only within the energy range of k_BT. The same arguement holds true for the tunneling rate through the tunnel junction 2.

The four inequalities in eq. 2.33 and eq. 2.34 along with the tunneling rates, eq. 2.31 and eq. 2.32 define the Coulomb blockade region. Coulomb blockade regions have a rhombic shape and the region within this rhombic shape is a stable state with an electron number n. Hence, this is refered to as a charge stability diagram. Due to the shape of the Coulomb blockade region it is also refered to as the "Coulomb diamond". The slopes of the edges of the Coloumb diamond are related to the capacitances.

To derive the relation between the slopes of Coulomb diamond, we first define the electrochemical potential of the island with n electrons on it which is given by [22]:

$$\mu_n = \frac{e^2}{2C_\Sigma} - e\varphi \tag{2.35}$$

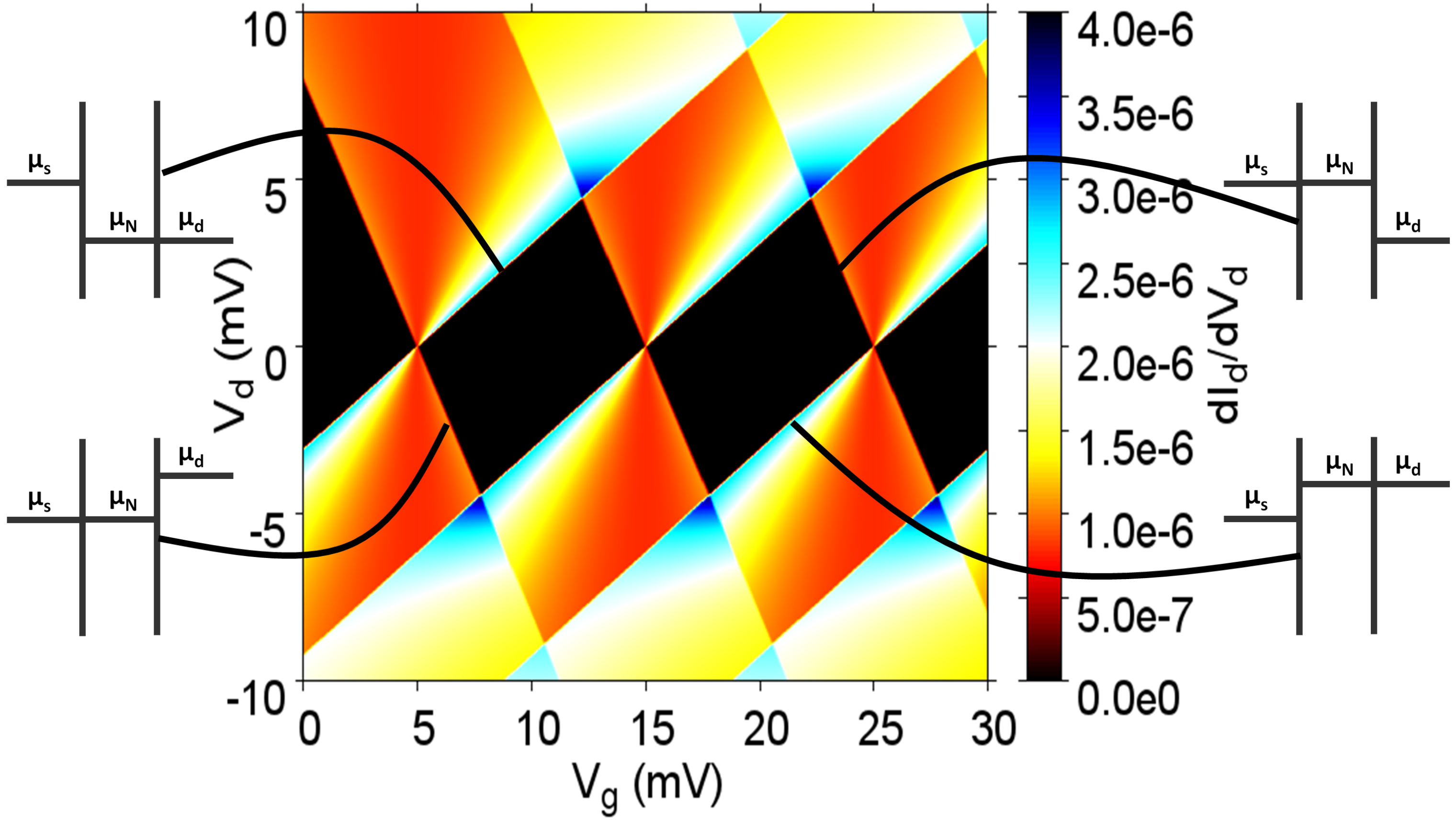

Figure 2.4: Simulated charge stability diagram or "Coulomb diamonds". The charge stability diagram shows the region with stable charges. The charge in the charge stability diagram fluctuates along the edge of the diamonds. The inset shows the schematic explanation of the alignment of the electrochemical potential on the island and the electrodes along the edges of the Coulomb diamonds.

where φ is the potential of the island given by $\varphi = \frac{(C_1V+C_2V+C_gV_g-ne)}{C_\Sigma}$.

We define the electrochemical potential of the source and the drain as μ_s and μ_d. The positive slope of the Coulomb diamond corresponds to the electrochemical potential of the island aligning with the electrochemical potential of the drain:

$$\mu_d = \mu_n$$

Therefore, for the case of bias applied on the drain and source grounded [23]:

$$\mu_d - eV = \frac{e}{C_\Sigma}\left(ne + \frac{e}{2} - C_2V - C_gV_g\right)$$

$$\left(-1 + \frac{C_2}{C_\Sigma}\right)V = \frac{e}{C_\Sigma}\left(n + \frac{1}{2}\right) - \frac{C_g}{C_\Sigma}V_g - \frac{\mu_d}{e}$$

$$-\frac{(C_1 + C_g)}{C_\Sigma}V = \frac{e}{C_\Sigma}\left(n + \frac{1}{2}\right) - \frac{C_g}{C_\Sigma}V_g - \frac{\mu_d}{e}$$

Differentiating the above equation w.r.t V_g gives us the positive slope of the Coulomb diamond:

$$\left(\frac{dV}{dV_g}\right)^+ = \frac{C_g}{C_1 + C_g} \tag{2.36}$$

From eq. 2.36, it can be seen that a single island tunnel-coupled to the source and the drain and capacitively coupled to the gate, with the source grounded, has a positive slope always less than unity. The negative slope of the Coulomb diamond corresponds to the electrochemical potential of the island aligning with the electrochemical potential of the source electrode:

$$\mu_s = \mu_n$$

Since the source is grounded,

$$\mu_s = \frac{e}{C_\Sigma}\left(ne + \frac{e}{2} - C_2V - C_gV_g\right)$$

$$\frac{C_2}{C_\Sigma}V = \frac{e}{C_\Sigma}\left(n + \frac{1}{2}\right) - \frac{C_g}{C_\Sigma}V_g - \frac{\mu_s}{e}$$

Differentiating the above equation w.r.t V_g gives us the negative slope of the Coulomb diamond:

$$\left(\frac{dV}{dV_g}\right)^{-} = -\frac{C_g}{C_2} \tag{2.37}$$

Fig. 2.4 shows the simulated charge stability diagram or "Coulomb diamonds". The charge stability diagram shows the region with stable charges. The charge on the island is stable within the Coulomb diamond and fluctuates only along the edge of the Coulomb diamonds. The inset of fig 2.4 shows the schematic explanation of the alignment of the electrochemical potential of the island and the electrodes along the edges of the Coulomb diamonds. In fig. 2.4, a trace at $V_d \approx 0V$ gives a series of oscillations as a function of gate voltage V_g. These oscillations are known as Coulomb blockade oscillations. Coulomb blockade oscillations are a variation in the conductance as a function of the gate voltage. We assume that the island is metallic so that the energy levels in the island are equally spaced. Hence the Coulomb oscillations are periodic in the gate voltage and the energy needed to add n and $n+1$ electrons is same. From eq. 2.35, the electrochemical potential of the dot with n electrons can be written as (in the linear regime):

$$\mu_n = \frac{e}{C_\Sigma}\left(ne + \frac{e}{2} - C_g V_g\right)$$

Using the condition $\mu_{n,V_g} = \mu_{n+1,V_g+\Delta V_g}$, we can find the distance between the consecutive Coulomb oscillation [11]:

$$\frac{e}{C_\Sigma}\left(ne + \frac{e}{2} - C_g V_g\right) = \frac{e}{C_\Sigma}\left((n+1)e + \frac{e}{2} - C_g(V_g + \Delta V_g)\right)$$

$$\frac{eC_g\Delta V_g}{C_\Sigma} = \frac{e^2}{C_\Sigma}$$

$$\Delta V_g = \frac{e}{C_g} \tag{2.38}$$

Eq. 2.38 allows us to calculate the gate capacitance from the spacing between the Coulomb oscillations.

We now consider the temperature dependence of the line shape of the Coulomb oscillation. For simplicity here, we assume that the tunneling rate through each barrier is equal $\Gamma_1 = \Gamma_2 = \Gamma$. In the limit, $\Gamma \ll k_B T$, the Coulomb oscillations are thermally broadened whereas in the limit $\Gamma \gg k_B T$ the Coulomb oscillations are broadened by the tunnel coupling. In order to see a Coulomb blockade charging effect , the temperature must be smaller than the charging energy of the island, $k_B T \ll \frac{e^2}{C_\Sigma}$. In the high temperature limit, $k_BT \gg \frac{e^2}{C_\Sigma}$, the conductance through the island is independent of the electron number and the size of the island. In the high temperature limit, the total conductance can be written as ohmic sum of the conductance through each barrier [11]:

$$\frac{1}{G} = \frac{1}{G_\infty} = \frac{1}{G_1} + \frac{1}{G_2} \tag{2.39}$$

where G_1 and G_2 are the conductance through the tunnel junctions 1 and 2 respectively and G is the total conductance.

Here we consider a metallic regime where the thermal energy is greater than the tunneling and the energy level spacing in the island but not greater than the charging energy of the island:

$$\Gamma, \Delta E \ll k_BT \ll \frac{e^2}{C_\Sigma} \tag{2.40}$$

In the metallic regime, the width of the Coloumb peak increases linearly with temperature, and the maximum conductance is $G_{max} = \frac{G_\infty}{2}$, half the high temperature value and independent of temperature. The factor $\frac{1}{2}$ is due to the fact that the electron on the island must first tunnel off before the next electron can tunnel onto it. This reduces the tunnel probability to half. The line shape of an individual conductance peak is given by [11][24]:

$$\frac{G}{G_{max}} = \frac{\frac{\delta}{k_BT}}{\sinh\left(\frac{\delta}{k_BT}\right)} \approx \cosh^{-2}\left(\frac{\delta}{2.5k_BT}\right) \tag{2.41}$$

where δ is the measured distance to the center of the conductance peak in units of energy. This can be expressed in terms of the gate voltage as $\delta = e\alpha. \mid V_g - V_{g,centre} \mid$ where $V_{g,centre}$ is the gate voltage at the center of the conductance peak and $\alpha = \frac{C_g}{C_\Sigma}$ is the lever arm parameter which tells us how well the gate is capacitively coupled to the island. From eq. 2.41, we can conclude that the Coulomb oscillations are more clearly visible with a decreasing temperature and hence, as the ratio $\frac{k_BT}{\frac{e^2}{C_\Sigma}}$ becomes smaller, the Coulomb oscillation peaks becomes more pronounced.

The lever arm parameter α also links the peak spacing as a function of gate voltage to the energy scale [25]:

$$\Delta E = \alpha \Delta V_g = \frac{eC_g\Delta V_g}{C_\Sigma} \tag{2.42}$$

The lever arm parameter α also connects to the slopes of the Coulomb diamond by the following relation [23]:

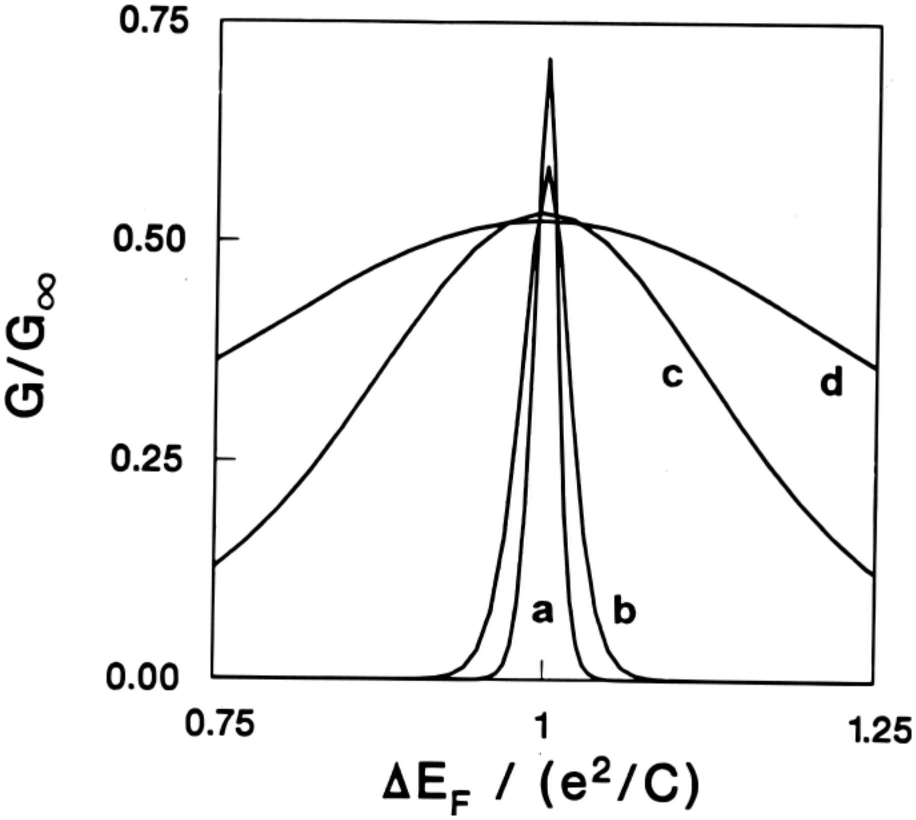

Figure 2.5: Line shape of the Coulomb oscillation as a function of temperature where a and b show the resonant tunneling regime where both the width and the amplitude of the Coulomb oscillation depend on temperature whereas c and d show the classical regime where only the width of the Coulomb oscillation depends on the temperature. This figure is taken from ref.[11] .

$$\mid \Delta m \mid = \frac{1}{\alpha} \tag{2.43}$$

where Δm is the difference in the two slopes of the Coulomb diamond.

2.4 Master Equation

The current flowing through the device due to electron tunneling onto and off the island can be calculated using the master equation technique. The change of charge e on and off the island can be described by the master equation given by [26]:

$$\frac{\partial \rho \left(n,t\right)}{\partial t} = \rho \left(n+1\right) \left[\Gamma_2^+ \left(n+1\right) + \Gamma_1^- \left(n+1\right)\right] - \rho \left(n\right) \left[\Gamma_2^- \left(n\right) + \Gamma_1^+ \left(n\right)\right] \tag{2.44}$$

where n is the number of electrons on the island t is the time and $\rho\left(n\right)$ is the probability of finding n electrons on the island.

To calculate the dc characteristics, a steady state solution of the eq. 2.44 is needed, which can be obtained by setting the above equation equal to zero. Therefore the eq. 2.44 becomes:

$$\rho \left(n\right) \left[\Gamma_2^- \left(n\right) + \Gamma_1^+ \left(n\right)\right] = \rho \left(n+1\right) \left[\Gamma_2^+ \left(n+1\right) + \Gamma_1^- \left(n+1\right)\right] \tag{2.45}$$

Eq. 2.45 tells us that in steady state, the possibility of a transistion from state $n+1$ to state n is equal to the possibility of a transistion from n to $n+1$. It is necessary to calculate $\rho\left(n\right)$ for all the possible charge states n. By substituting $n = -\infty \,\text{to}\, \infty$ in eq. 2.45 we calculate all the possible values of $\rho\left(n\right)$ as follows:

$$\rho \left(-\infty\right) \left[\Gamma_2^- \left(-\infty\right) + \Gamma_1^+ \left(-\infty\right)\right] = \rho \left(-\infty+1\right) \left[\Gamma_2^+ \left(-\infty+1\right) + \Gamma_1^- \left(-\infty+1\right)\right]$$

$$\rho \left(-1\right) \left[\Gamma_2^- \left(-1\right) + \Gamma_1^+ \left(-1\right)\right] = \rho \left(0\right) \left[\Gamma_2^+ \left(0\right) + \Gamma_1^- \left(0\right)\right]$$

$$\rho \left(0\right) \left[\Gamma_2^- \left(0\right) + \Gamma_1^+ \left(0\right)\right] = \rho \left(1\right) \left[\Gamma_2^+ \left(1\right) + \Gamma_1^- \left(1\right)\right]$$

$$\rho \left(\infty-1\right) \left[\Gamma_2^- \left(\infty-1\right) + \Gamma_1^+ \left(\infty-1\right)\right] = \rho \left(\infty\right) \left[\Gamma_2^+ \left(\infty\right) + \Gamma_1^- \left(\infty\right)\right]$$

In order to solve the above equations, $\rho\left(n\right)$ must satisfy the boundary condition given by:

$$\rho\left(n\right)\rightarrow 0\,as\,n\rightarrow\pm\infty \tag{2.46}$$

Using the boundary condition in eq. 2.46, all the values of $\rho\left(n\right)$ can be calculated. The normalization condition for $\rho\left(n\right)$is:

$$\sum_{n=-\infty}^{\infty}\rho\left(n\right)=1 \tag{2.47}$$

For this, the following transformation is needed:

$$\rho\left(n\right)\rightarrow\frac{\rho\left(n\right)}{\sum_{n=-\infty}^{\infty}\rho\left(n\right)} \tag{2.48}$$

Finally, current can be calculated by:

$$I\left(V\right)=e\sum_{n=-\infty}^{\infty}\rho\left(n\right)\left[\Gamma_1^+\left(n\right)+\Gamma_1^-\left(n\right)\right] \tag{2.49}$$

Here the current $I(V)$ is expressed as a multiplication of probability and tunneling rate onto and off the island which gives the net current across tunnel junction 1.

The expression be similarly written for tunnel junction 2:

$$I\left(V\right)=e\sum_{n=-\infty}^{\infty}\rho\left(n\right)\left[\Gamma_2^+\left(n\right)+\Gamma_2^-\left(n\right)\right] \tag{2.50}$$

This method is used in this work to calculate the current through the device. The simulation program is written in Python by Matthieu Pierre (CEA-INAC Grenoble).

2.5 Coulomb Staircase

The $I-V$ characterisic of the SET at a given gate voltage V_g shows a Coulomb gap at a low bias voltage V (i.e. $eV<\frac{e^2}{C}$). This Coulomb gap represents a stable charge region on the island. The charge on the island can be changed either by changing the gate voltage at fixed bias voltage, which moves the electrochemical potential of the island within the transport window, or at a fixed gate voltage, the bias voltage can be changed. Here we consider the case of sweeping the bias voltage at fixed gate voltage. In the case where both the tunnel barriers have equal resistance $R_1=R_2$, for smaller

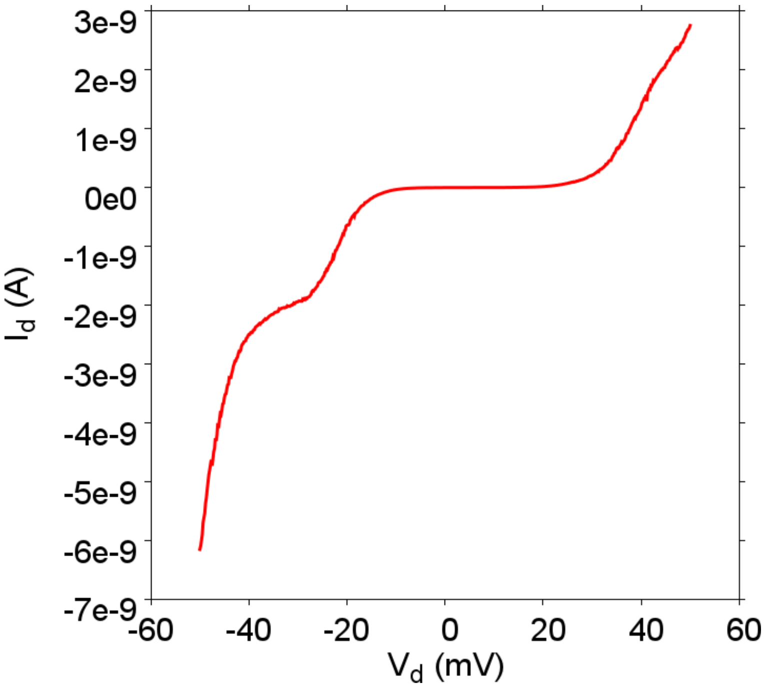

Figure 2.6: Coulomb staircase in current as a function of bias voltage arising from asymmetric tunnel resistances of the tunnel barrier is exhibited.

bias voltages, there is a Coulomb gap and the current through the device increases linearly with increase in bias voltage. The increase in current outside the Coulomb gap region depends on the tunneling resistances of the tunnel junctions, R_1 and R_2 respectively. If the tunnel resistances R_1 and R_2 have very different values from each other then the tunneling rates Γ_1 and Γ_2 alo have very different values and the current increases in step-like manner often refered to as the “Coulomb staircase”. Each step in the Coulomb staircase represents an electron added or removed from the island. For $R_1 \ll R_2$, at sufficiently high positive bias voltage where the Coulomb blockade is overcome, an electron leaving the island via tunnel junction 2 is immediately replaced by another electron through the junction 1. Whereas for the case when the polarity of the bias voltage is reversed, an electron entering the island via tunnel junction 2 leaves quicker through junction 1 than the next electron entering the island via tunnel junction 2. This leads to a rise in current in a step-like manner giving rise to the Coulomb staircase. Fig. 2.6 demonstrates the Coulomb staircase due to asymmetric tunnel rates across the tunnel barriers.

2.6 Quantum Dots

So far in the discussion we have considered charging effects in a metallic island, where a number of free electrons already existed on the island and the spacing between the energy levels on the island were much smaller than the thermal energy and charging energy of the island:

$$\Delta E < k_B T < E_c \tag{2.51}$$

If the island is made small enough so that the fermi wavelength of the electrons confined within the island is comparable to the dimensions of the island, then the island can be considered as a particle-in-a-box where the electron occupies discrete energy levels on the island. Such an island is referred to as a quantum dot [27][28]. Quantum dots have a discrete energy spectrum and the spacing between the energy levels is greater than the thermal energy:

$$\Delta E > k_B T \tag{2.52}$$

If such a quantum dot is connected to electron reservoirs via tunnel barriers, then the conductance through the dot depends on the quantum confinement and on single electron effects. Due to the discrete number of electrons and the discrete energy spectrum of the quantum dots, they are sometimes reffered to as “artificial atoms” [28]. The energy spectrum of the quantum dot can be measured by doing transport spectroscopy.

We consider a quantum dot confined in all the three dimensions with each side having dimension L_x, $L_y\, and\, L_z$ along the $x-, y-$ and $z-axis$. Due to confinement along all the three directions, the quantum dot behaves as a 3-D potential well and the energy levels in the dot are given by [29]:

$$E_{n_x,n_y,n_z} = \frac{\hbar^2\pi^2}{2m^*}\left(\frac{n_x^2}{L_x^2} + \frac{n_y^2}{L_y^2} + \frac{n_z^2}{L_z^2}\right) \tag{2.53}$$

where n_x, $n_y\, and\, n_z$ are the quantum numbers along the $x-, y-$ and $z-axis$ and m^* is the effective mass. The spacing between the energy levels (ΔE) for a box with dimension L confined either 1-D, 2-D or 3-D, is given by [11]:

For 1-D:

$$\Delta E = \left(\frac{n}{4}\right)\frac{\hbar^2\pi^2}{m^*L^2} \tag{2.54}$$

For 2-D:

$$\Delta E = \left(\frac{1}{\pi}\right)\frac{\hbar^2\pi^2}{m^*L^2} \tag{2.55}$$

For 3-D:

$$\Delta E = \left(\frac{1}{3\pi^2 n}\right)^{\frac{1}{3}}\frac{\hbar^2\pi^2}{m^*L^2} \tag{2.56}$$

The energy scale of the level spacing is given by $\frac{\hbar^2\pi^2}{2m^*L^2}$. The level spacing increases linearly with n in $1-D$, remains constant in $2-D$ and decreases in $3-D$ with an increase in n.

We assume that a quantum dot is small enough so that the level spacing is greater than the thermal energy but smaller than the charging energy:

$$k_BT < \Delta E < E_c \tag{2.57}$$

Furthermore, we assume that a small bias voltage is applied across the device so that eV_d is smaller than ΔE and $\frac{e^2}{C_\Sigma}$ to ensure the transport of electrons takes place in the linear regime i.e. $\mu_s \approx \mu_d$. For a given gate voltage V_g, the electrochemical potential of the quantum dot is given by [11]:

$$\mu_n = E_n + \frac{\left(n-\frac{1}{2}\right)e^2}{C_\Sigma} - \frac{C_gV_g}{C_\Sigma}e \tag{2.58}$$

where n is the number of electrons on the dot, E_n is the energy of the n^{th} confined level, and the second term is the energy needed to add n electrons on the dot sweeping the gate voltage. Using eq. 2.58, the energy needed to charge the quantum dot with one electron can be calculated, and is also known as the addition energy. The addition energy is given by the difference in the electrochemical potential for $n+1$ and n electrons on the dot:

$$\mu_{n+1} - \mu_n = E_{n+1} + \frac{\left((n+1)-\frac{1}{2}\right)e^2}{C_\Sigma} - \frac{C_gV_g}{C_\Sigma}e - E_n + \frac{\left(n-\frac{1}{2}\right)e^2}{C_\Sigma} - \frac{C_gV_g}{C_\Sigma}e$$

$$= \Delta E + \frac{e^2}{C_\Sigma} \tag{2.59}$$

The Coulomb blockade can be overcome by sweeping the gate voltage. With an increase in the gate voltage, μ_{n+1} is lowered until it enters the transport window, then an electron jumps from source to dot and from dot to drain. The period of Coulomb oscillations can be obtained by using eq. 2.58 and by using the condition:

$$\mu_{n+1}(n+1, V_g + \Delta V_g) = \mu_n(n, V_g)$$

$$E_{n+1} + \frac{\left((n+1)-\frac{1}{2}\right)e}{C_\Sigma} - \frac{C_g(V_g+\Delta V_g)}{C_\Sigma}e = E_n + \frac{\left(n-\frac{1}{2}\right)e}{C_\Sigma} - \frac{C_gV_g}{C_\Sigma}e$$

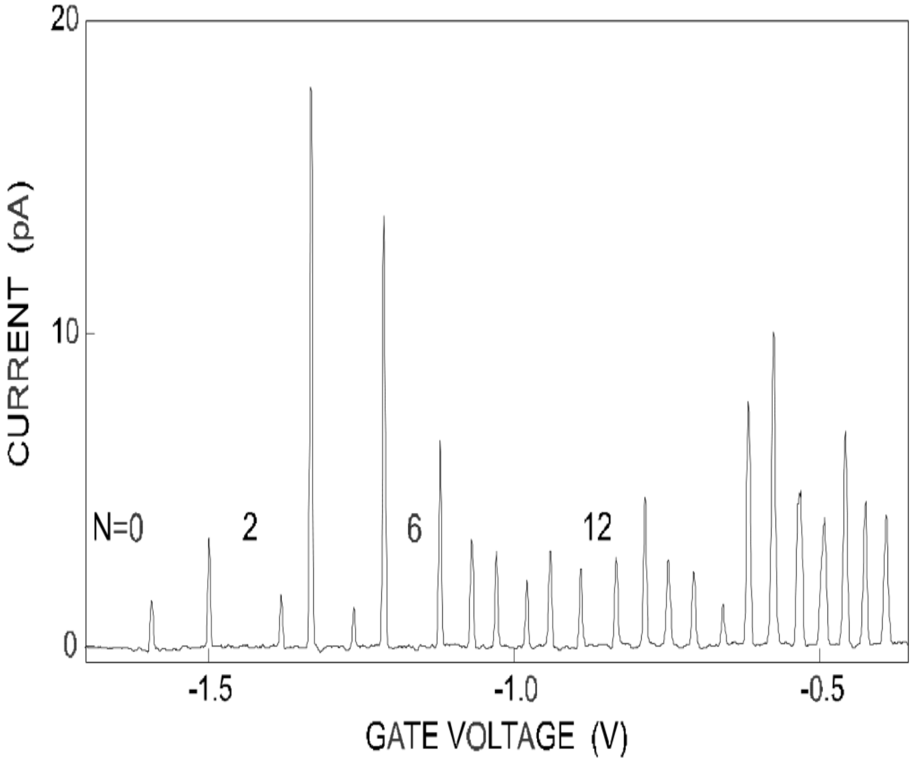

Figure 2.7: Coloumb oscillations in a current as a function of gate voltage. Aperiodic spacing between the peaks and irregular peak height is a typical feature of a quantum dot which is exhibited in the Coloumb oscillations shown. This figure is taken from ref.[11].

$$\Delta V_g = \frac{C_\Sigma}{eC_g}\left(\Delta E + \frac{e^2}{C_\Sigma}\right) \tag{2.60}$$

The period of oscillations in a quantum dot depends on the charging energy $\left(\frac{e^2}{C_\Sigma}\right)$ and spacing between the energy level (ΔE). The spacing between the energy level is often not constant and varies from level to level. This leads to aperiodic Coulomb oscillations. In a metallic SET, the Coulomb oscillations have a similar peak height, whereas the peak height of the Coulomb oscillations in quantum dots varies. This is due to the fact that each Coulomb oscillation is associated to a particular energy level. The shape of the electron wavefunction on each energy level is different. The tunneling probability of each electron depends on the electron wavefunction of that particuar energy level. This affects the tunnel probability of the electron on each level in the quantum dot and hence the height of the Coulomb oscillations varies. It should be noted that irregular peak heights could occur due to several reasons and not necessarily arise from a quantum confinement. For the silicon MOSFET devices which turn into a SET at low temperature, the tunnel barriers are affected by the gate bias [30] which could result in irregular peak heights. Fig. 2.7 shows typical Coulomb oscillations in quantum dots.

The conductance as a function of $V_d - V_g$ generates a Coulomb diamond like in the case of the metallic SET. In fig. 2.8, in addition to the Coulomb diamond there are conductance lines running along the edges of the Coulomb diamonds. These lines correspond to excited states aligning with the electrochemical potential of the source and the drain in the non-linear regime. These discrete excited states have an energy level separation greater than the thermal energy. Fig. 2.8 shows the simulated Coulomb diamond for a quantum dot with excited states separated from the ground state by 10, 15 and $17 meV$ at $T = 1K$. Fig. 2.9 shows the schematic explanation of the alignment of the energy levels with the electrochemical potential of the source and the drain. Coulomb blockade in a SET can be overcome by two ways:

1. By changing the gate voltage which moves the energy levels of the quantum dot within the transport window in a linear regime (giving a series of oscillation in fig. 2.8 at $V_d = 0V$)
2. By sweeping the bias voltage for a fixed gate voltage.

Since the energy levels in the quantum dot move linearly as a function of bias voltage V and gate voltage V_g, we get a set of lines in the non-linear measurement which forms the Coulomb diamond. At $V_g = 0V$, if the ground state in the quantum dot does not align with the electrochemical potential of the source and drain $(V_d \sim 0V)$, then a finite gate voltage is needed to push the ground state of the quantum dot within the transport window which is marked by *a* in fig. 2.8 which appears at $V_g \sim 5mV$. Fig. 2.9a schematically demonstrates the alignment of the energy level in the quantum dot with the electrochemical potential of the source and the drain. The application of positive voltage on the gate electrode linearly lowers the ground state and the excited states in the quantum dot. The positive slope of the Coulomb diamond corresponds to the energy level in the quantum dot aligning with the electrochemical potential of the drain. One point of such an alignment is shown for a positive bias and is marked as *b* in fig. 2.8. Fig 2.9b schematically demonstrates, the origin of such a situation. Similarly, the negative slope corresponds to the energy level in the quantum dot aligning with the electrochemical potential of the source. One point for such an alignment is shown for negative bias and is marked by *c* in fig. 2.8. Fig.2.9c shows this situation schematically. At point *d* in fig.2.8, there is an intersection of lines with positive and negative slope. At this point, the ground state in the quantum dot aligns with the electrochemical potential of the drain, which gives rise to a positive slope. Whereas the first excited state in the quantum dot aligns with the electrochemical potential of the source, which gives rise to a negative slope. This is shown schematically in fig. 2.9d. Similarly, at point *e* in fig. 2.8 the ground state in the quantum dot aligns with the electrochemical potential of the source and the first excited state aligns with the electrochemical potential of the drain. Likewise, all the lines running along the edge of the next Coulomb diamonds can be explained with a similar argument.

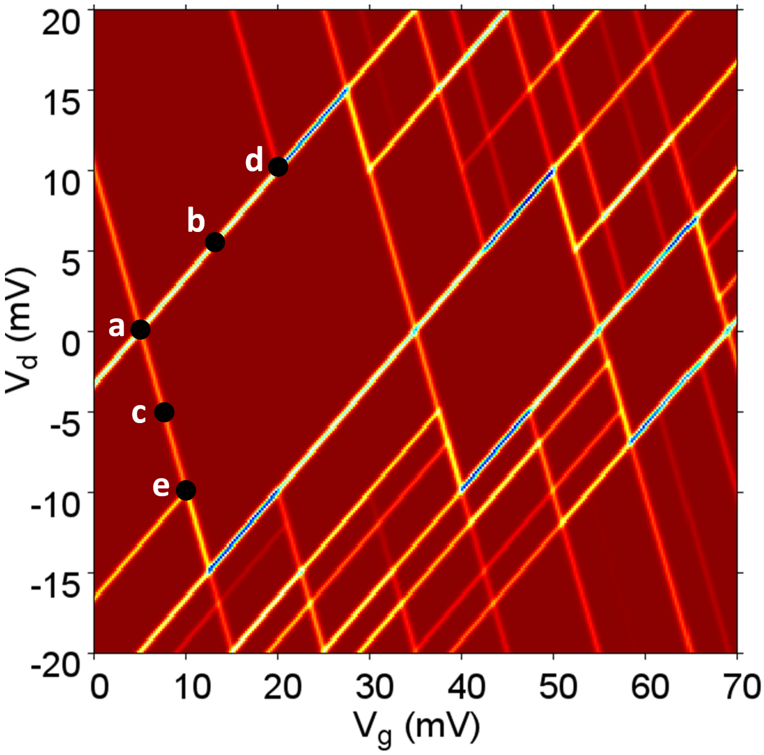

Figure 2.8: Simulated Coulomb diamond for quantum dot. Clearly, excited states are visible running along the edges of the Coulomb diamonds. Excited states are separated from the ground state by 10, 15 and $17meV$ at $T = 1K$. Source, drain and gate capacitances used for simulation are $8aF$, $8aF$ and $16aF$ respectively.

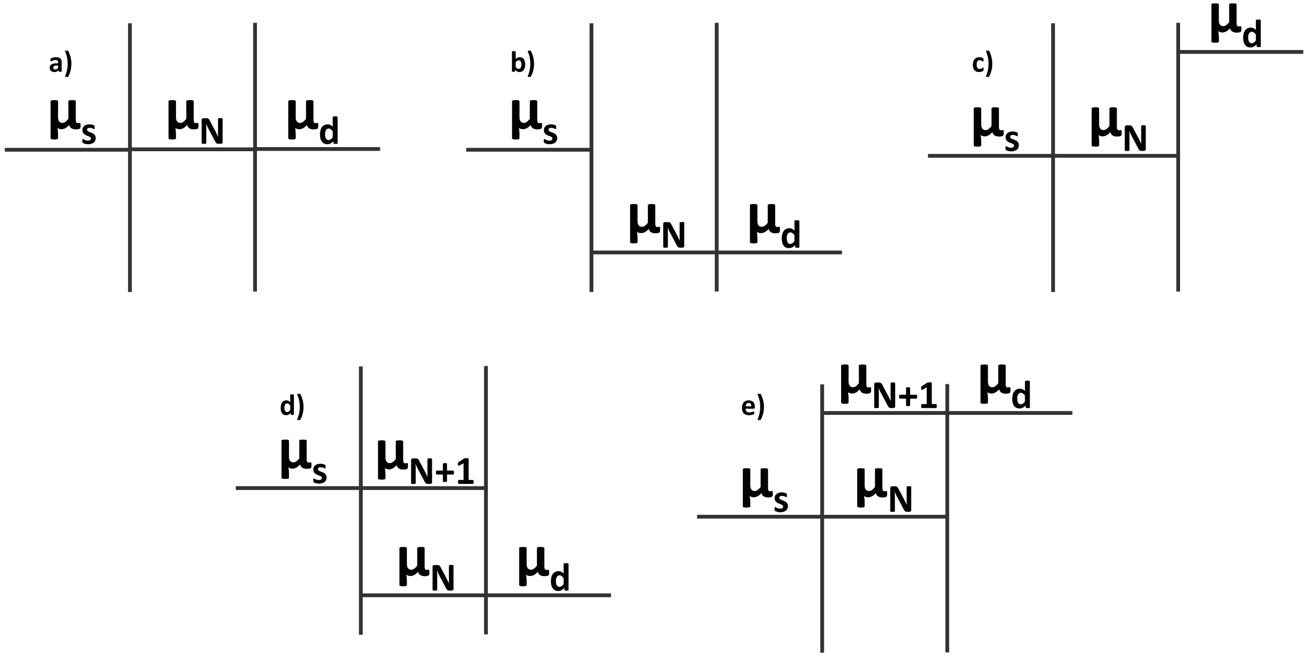

Figure 2.9: Schematic explanation of the ground state and the excited states aligning with the electrochemical potential of the source and drain leads. a) Ground state of the dot aligning with the electrochemical potential of the source and drain. If at $V_g = 0V$, the ground state does not align with the source and drain, then this situation occurs at finite gate voltage. b) Ground state aligning with drain for positive drain voltage representing the situation at b in simulation. c) Ground state aligning with source representing the situation at c in simulation. d) and e) show ground state and excited state aligning with drain and source respectively, representing the situation at d and e respectively in simulation.

Chapter 3

Fabrication, Sample Preparation and Experimental Set-up

3.1 Introduction

SETs and coupled dot systems have been studied and demonstrated in the past [11][28]. With that being said, AFSID project aims to study the problem of variability in the nanotransistors and SET as a promising candidate towards the end of ITRS roadmap. In order to implement SET in the industry, the fabrication process should be compatible with the industrial CMOS technology and SETs should work at room temperature. The devices faricated in the work are compatible with the existing CMOS technology. The dimensions of the devices are small enough to give us the hope that these devices can work at higher temperatures (much higher temperatures than $4.2K$). The devices measured in this work are fabricated on a large scale. On a 8 inch wafer, several hundreds of devices were fabricated with different dimensions and different geometry [31]. In this project we have tried to show that the mass production of silicon SETs can be done [32]. In this chapter we discuss briefly the fabrication process followed by the sample preparation and the measurement set-up used.

3.2 Fabrication

The nanowire transistors used in this thesis are fabricated for the project Atomic Functionalities on Silicon Devices (AFSID) [7]. The fabrication of the devices was done at the Partner site at CEA Leti Grenoble [33]. The process flow has been kept as close as possible to the standard Fully Depleted Silicon On Insulator (FDSOI) integration. The complete flow chart of the process is shown in fig. 3.1 below.

In a standard Silicon on Insulator (SOI) substrate, the silicon above the buried oxide is typically $200nm$. This active layer is then thinned down to the desired thickness. In this work, devices with different silicon thickness were produced. Three batches of samples were produced. In the first batch a silicon thickness of $20nm$ was used. In the pre-second batch, a silicon thickness of $10nm$ was used. Whereas in the second batch silicon thicknesses of $12nm$ and $8nm$ were used. This thinning of the silicon thickness is done in two steps. First, the thickness of the active layer is reduced to $70nm$ by oxidation at 1050° C under $O_2 + HCl$. Then a second oxidation process is done to

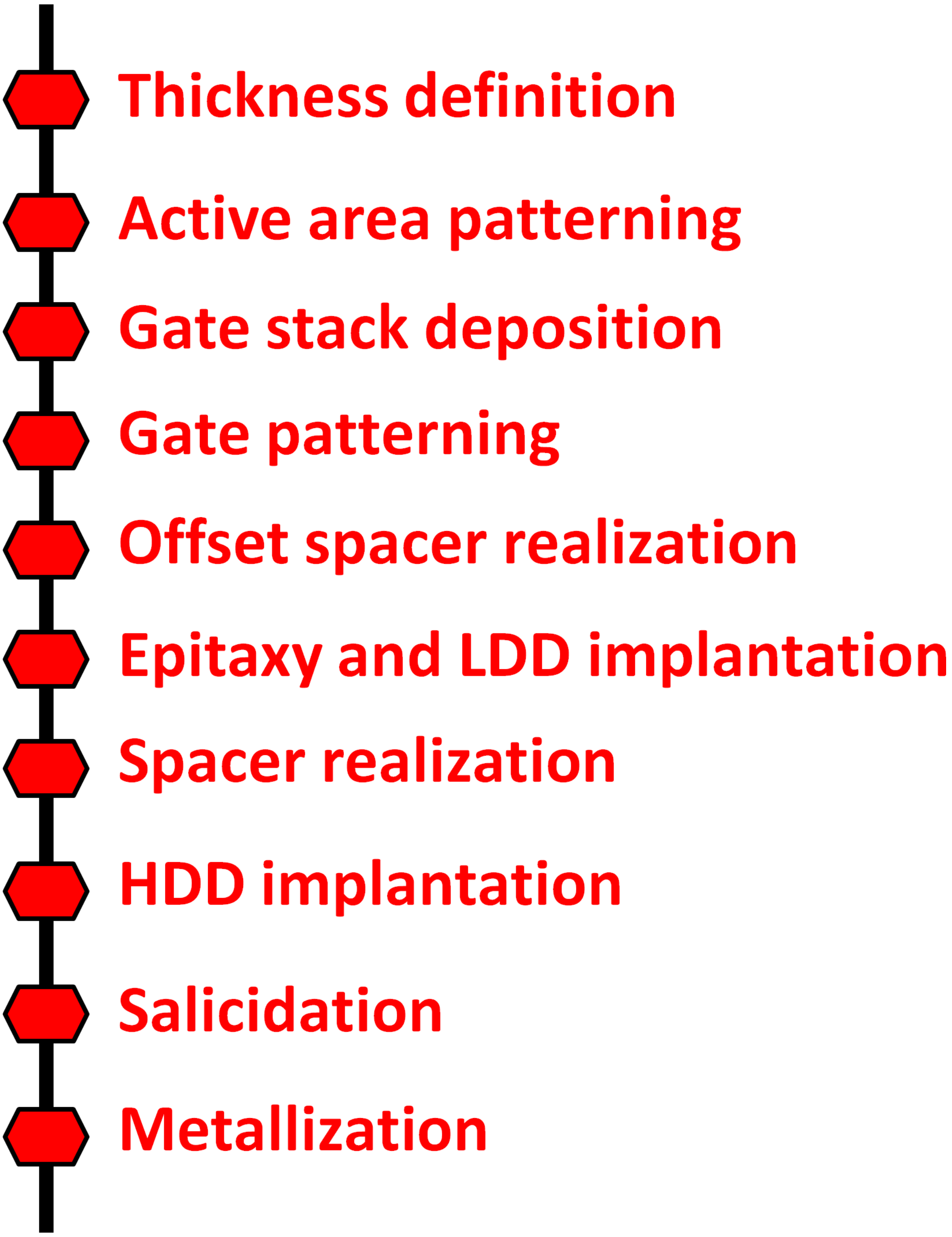

Figure 3.1: Flowchart of the complete fabrication process.

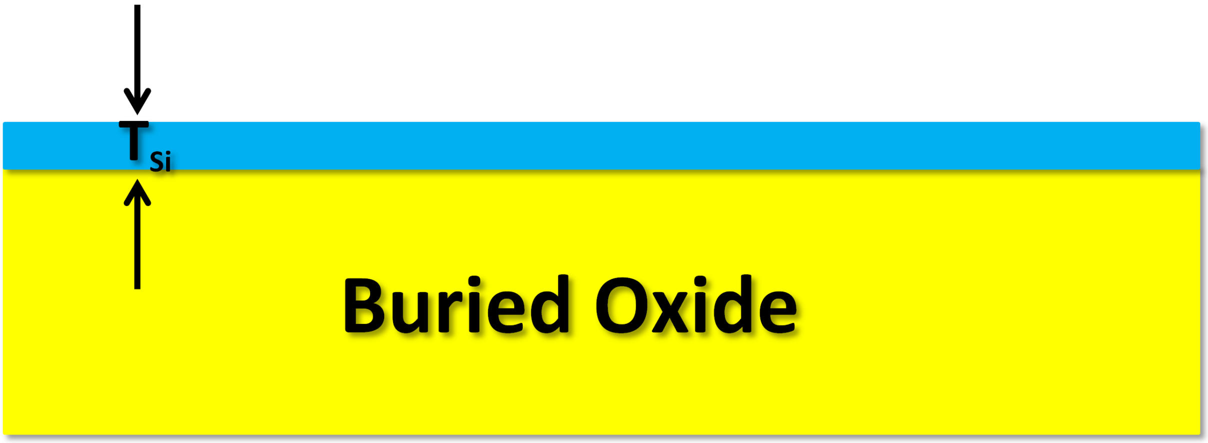

Figure 3.2: Active silicon layer on top of the Burried Oxide (BOX).

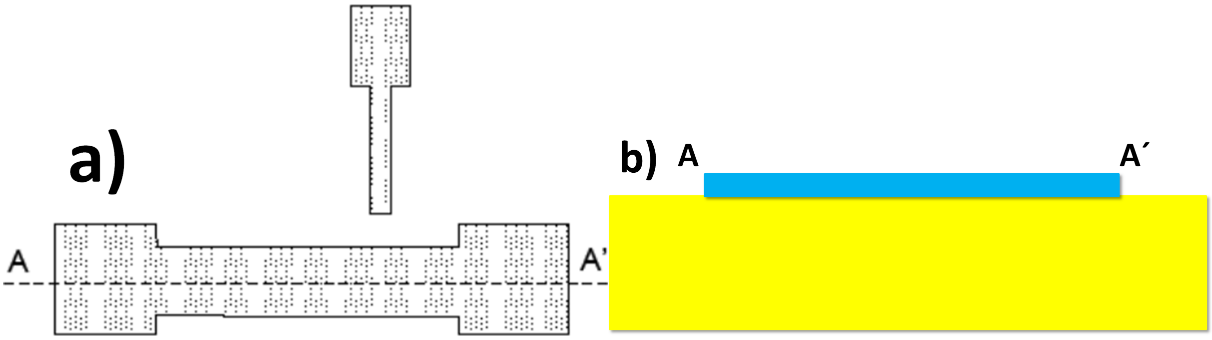

Figure 3.3: a) Active layer etched out after the e-beam lithography. b) Cross section along the line A-A´ in fig. 3.3a.

reduce the active layer thickness to $20nm$,$12nm$, $10nm$ or $8nm$ thick, depending on the desired thickness. The active layer thickness of $70nm$, which is achieved after the first oxidation process is used to define the contacts whereas the active layer thickness acheived after the second oxidation is used to define the channel. Fig. 3.2 shows the active layer after the second oxidation process which is used to define the channel region. In all the figures describing the fabrication process, we show only the active layer after the second oxidation process and the regions with an active layer of $70nm$ which define the contacts are not shown.

The lithography works with negative tone resist. The active area is patterned by the electron beam (channel region), whereas in the common areas (contact pads, etc.), deep ultravoilet (DUV) lithography is done. Fig. 3.3 shows the nanowire etched out after the e-beam lithorgraphy.

Next, the gate stack is formed. The gate stack is composed of $5nm$ of thermal SiO_2 and $50nm$ of in situ n^+ doped polysilicon (fig. 3.4).

For the gate patterning, the lithography technique adopted is the same as for the active layer. First, a low dose implantation can be done after the gate etching. Since the aim within the AFSID project is to form a quantum dot (artificial atom) in undoped silicon, at this stage Lightly Doped Drain (LDD) is avoided. In order to form an undoped artificial atom, silicon nitride spacers (Si_3N_4) are deposited around the gate (green line

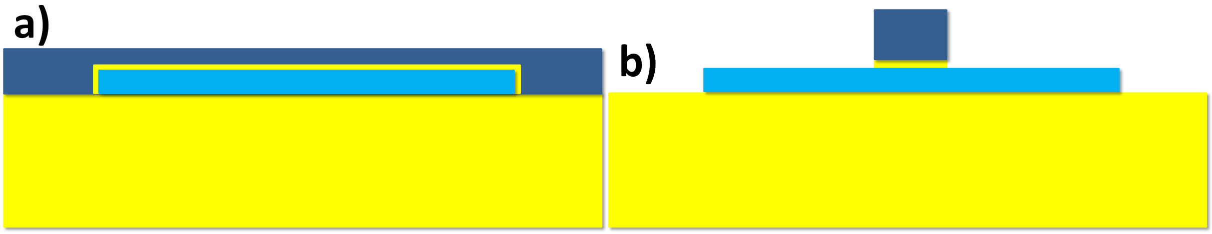

Figure 3.4: a) Gate stack consisting of SiO_2 and n^+ polysilicon. b) The formation of the gate along with the gate oxide.

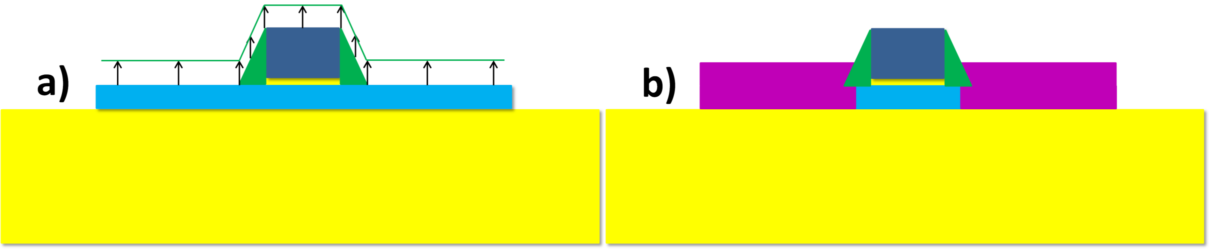

Figure 3.5: a) Realization of spacer around the gate. b) Epitaxy and HDD implantation.

passing around the top edge of the arrow in fig. 3.5a). Silicon nitride spacers are removed by the etching process. Due to equal etching rates from all the sides, the etching process removes a certain thickness of silicon nitride layer from all the sides (height of the arrows in fig. 3.5a). This process removes all the material on the horizontal surfaces while leaving material on the sidewalls of the gate which defines the final spacer thickness $t_{spacers}$ (dark green region in fig. 3.5a). Different thicknesses of the silicon nitride spacers were used. In the first batch, a silicon nitride thickness of $40nm$ was used, whereas in the second batch a more complex spacer pattern was implemented. In some wafers, spacers of $15nm$ thickness were used and in other wafers, spacers of $25nm$ thickness were deposited in two steps. These spacers along with the gate electrode serve as a mask which protects the channel below the gate from the next step of source-drain implantion. Hence, the channel below the gate is very low doped. The doping level in the channel also depends on the spacer thickness.

To optimize the access resistance, epitaxy was performed by increasing the silicon thickness above the BOX. Source-drain implantion (Highly Doped Drain or HDD) and an activation annealing is then performed (fig. 3.5b). Doping the source and drain access regions is a very critical process for thin SOI layers for two reasons:

1. High doping levels are needed to obtain sufficient conductance, especially at low temperature where the dopants freeze out if the doping is too low
2. If the defect level after doping is beyond $5 * 20^{21} cm^{-3}$, the active layers remain amorphous after annealing rather than recrystallizing.

3.3 SEM and TEM Analysis of the Devices

One of the important tasks in this work is to fabricate SETs operating as arficial atoms in undoped silicon at a temperature above $4.2K$. The thermal energy corresponding

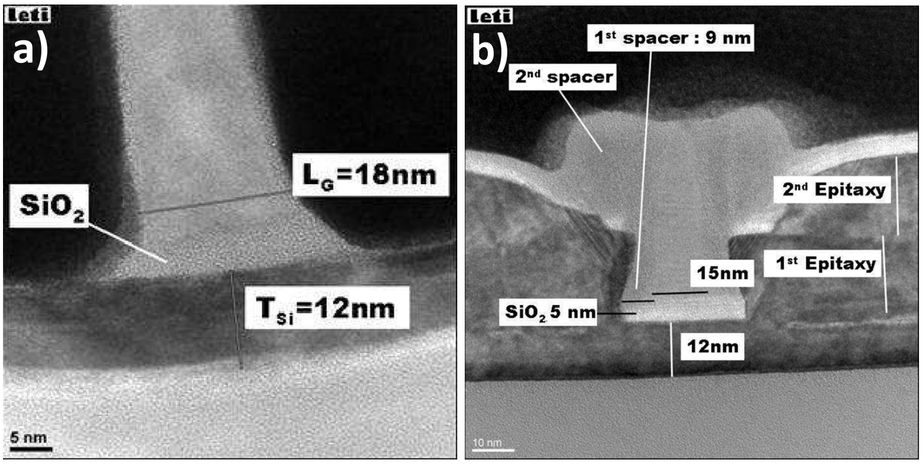

Figure 3.6: a) Isolated gate of a 20*nm* device with trimming process. Gate length measured is 18*nm*. b) Isolated gate of a 20*nm* device at the end of the process (without back-end). Very aggressive gate length of 15*nm* has been achieved [Images received from Leti].

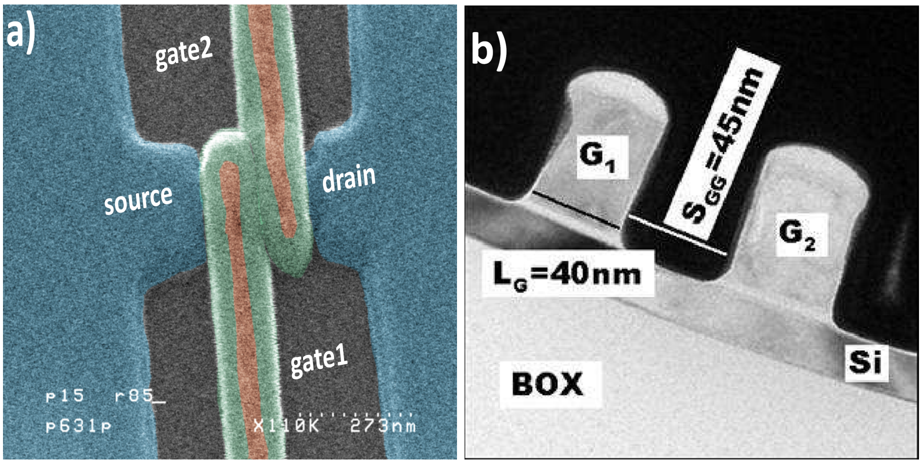

Figure 3.7: a) Colored SEM top view showing a nanowire with two gates and 40*nm* thick spacers. Blue is SOI, red is poly-silicon gate and green are nitride spacers. b) Two gates in series after gate etching (no trimming of resist have been performed). The pitch resolved here is 85*nm* [Images received from Leti].

to $4.2K$ is $0.36meV$. In order for the devices to work at a temperature above $4.2K$, the charging energy must be well beyond $0.36meV$. For this reason the devices should have a total capacitance smaller than $4.4 \cdot 10^{-16}F$. Devices measured in this work have silicon thicknesses of $20nm$, $12nm$ and $8nm$. In addition, gate lengths as small as $15nm$ were achieved. Fig. 3.6a shows the TEM image of a single top gate device with a silicon thickness of $12nm$, gate length of $18nm$ and silicon dioxide of $5nm$ thickness. Fig. 3.6b shows another device with silicon thickness of $12nm$, gate length of $15nm$, a silicon dioxide of $5nm$ and uses a double spacer as mentioned in the previous section.

The fabrication process in the last section describes a simple device with a single top gate. In such a device with a single top gate, the region below the gate forms an artificial atom on application of positive voltage (see Chapter 4). Placing such two top gates in series can form an artificial molecule. One advantage of such devices is that they are more compact. Fig. 3.7a shows the colored SEM top view showing a nanowire with 2 gates and $40nm$ thick spacers. The color scheme in the fig. 3.7a is as follows: Blue is the SOI, red is the polysilicon gate and green are nitride spacers.

In this image, the region between the two gates is protected during the HDD, which keeps this region undoped. With small spacers, a small region is left open during the HDD which can form a third dot in the central region between the gates (see chapter 4: Triple Dots in Series). Such a configuration allows a compact device where three dots are tuned with only two gates. These coupled SETs present some advantages as compared to other silicon based coupled SETs [34]. They necessitate only two control gates (instead of four). A disadvantage of such a geometry is that individual control of the dots is not possible since each gate controls two dots. Fig. 3.7b is an illustration of a double gate device after gate etching. In fig. 3.7b we note the very good morphology of the double gated device, each gate is $40nm$ long and space between the gates is $45nm$. This pitch (sum of distance between the two gates and the gate length) of $85nm$ is “state-of-the-art”, and it is worth noting that the space between these gates is very well resolved after the gate etching.

In addition to single gate and double gate devices there are also some complex devices with a single top gate and two side gate geometry which give us additional freedom (see chapter 4 and chapter 5).

3.4 Sample Preparation

3.4.1 Dicing

Devices are fabricated on a 8-*inch* wafer. Each wafer consists of 12 dices and each dice consists of few hundred devices with different geometries and different dimensions. In order to measure these devices, the wafer is first covered with PMMA to protect the devices while dicing. Then each dice is separated by dicing the wafer, then these dices are further cut into smaller chips of appropriate size so that they can fit into the chip carriers.

Device Bonding

Before gluing the sample, it is rinsed in an acetone ultrasonic bath to remove any particles from the surface and to remove the PMMA resist which was spin coated over the wafer before dicing for protection. The chip is then glued into the chip carrier with insulating glue or conducting silver and then dryed on a hot plate for 30 mins at $90°C$. Connections from the device to the chip carrier are made using the Hymer hybond $572A$ [35]. Fig. 3.8 shows the Hymer hybond used to bond the wires. Parameters used for bonding the chip are given in the table below:

Fig. 3.9a shows the whole view of a chip glued into the chip carrier and the wires from the chip carrier going to the devices. Fig. 3.9b shows a closer view of the wires coming from the chip carrier bonded on the device bond pads.

	Ultrasonic power	Ultrasonic time	Force
1st	46	90	42
2nd	48	90	28

Table 3.1: Parameters used for bonding the device on the chip carrier.

Figure 3.8: Hymer hybond 572*A* used for bonding the devices on the chips to the chip carriers .

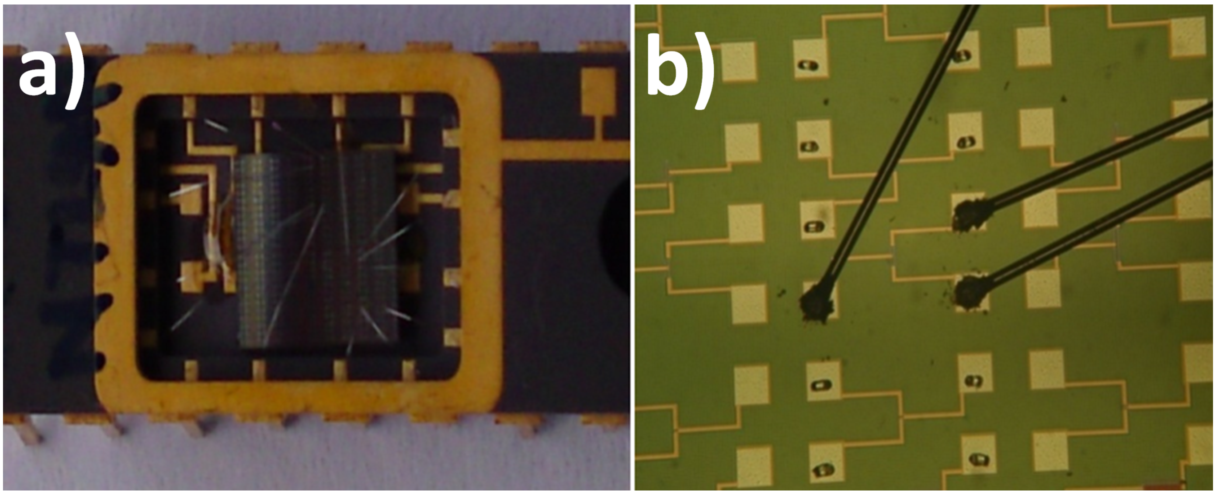

Figure 3.9: a) Chip glued into the chip carrier and the device bonded to the chip carrier. b) Closer look of the device bonded to the chip carrier.

3.5 Experimental Technique

3.5.1 Introduction

In order to study the physics of electron transport through such nanostructures, it is necessary to perform measurements at low temperatures. In this work measurements were initally done at room temperature and then the device was cooled down to $4.2K$ in a helium bath and in a dilution refrigerator. The dilution refrigerator used is an Oxford made Kelvinox ^{3}He/^{4}He which is capable of cooling the devices down to approximately $70mK$.

3.5.2 Dilution Refrigerator

The operating principle of the dilution refrigerator (fig. 3.10a) was first proposed by H. London in 1951 [36][37]. The main components of the dilution refrigerator are shown in fig. 3.10a. The whole fridge is immersed in a liquid helium bath at $4.2K$. Some of the liquid helium is drawn from this bath into the 1.5K pot. A vaccum pump is used to lower the pressure in the $1.5K$ pot resulting in lowering the temperature of the liquid to 1.5K. Then, the mixture, mainly ^{3}He gas coming from the pump at room temperature is pre-cooled to $4.2K$ by the liquid helium bath. This mixture is passed via a pipe through the $1.5K$ pot. As the mixture passes through the $1.5K$ pot, heat is drawn away from the mixture inside the pipe and the mixture condenses. This ^{3}He rich mixture drips into the still and the mixing chamber as a homogenous mixture. The mixture is not cooled enough to set-up phase boundary (fig. 3.10b) but only cools it down to $1.5K$. A second vaccum pump lowers the pressure in the still, inducing evaporation and resulting in further cooling of the liquid in the still. Since ^{3}He is lighter, ^{3}He evaporates more easily than ^{4}He. This leaves mainly ^{4}He in the still in the liquid form. This evaporation of ^{3}He starts the refrigeration cycle. The evaporated ^{3}He gas passes through the cold traps where this gas is purified and is funnelled into the condenser within the $1.5K$ pot. Inside this condenser the ^{3}He gas re-liquifies. A narrow capillary tube is located below the condenser which provides the flow impedence that maintains the pressure required to make the helium reliquefy. The ^{3}He passes through the heat exchangers which cools ^{3}He further down to within few millikelvin of the target temperature. The still and the mixing chamber are connected, so the liquid ^{3}He coming from the condenser is also added to the mixing chamber which mainly contains liquid ^{4}He which was funnelled into the chamber from the still at the beginning of the refrigeration cycle. At temperatures lower than $0.8K$, the ^{3}He/^{4}He mixture seperates into two layers [38], the upper layer mainly contianing lighter ^{3}He and lower layer mainly containing heavier ^{4}He and some ^{3}He. Since ^{3}He is evaporated from the still, this lowers the ^{3}He concentration in the still. In order to restore the equilibrium concentration again in the still, the ^{3}He drives from the lower phase of the mixing chamber up into the still. This in turn disturbs the equilibrium in the lower phase of the mixing chamber. In order to restore the concentration of ^{3}He in the lower phase of the mixing chanber, ^{3}He atoms cross over to the bottom layer. In this way, the continuous flow of ^{3}He provides cooling.

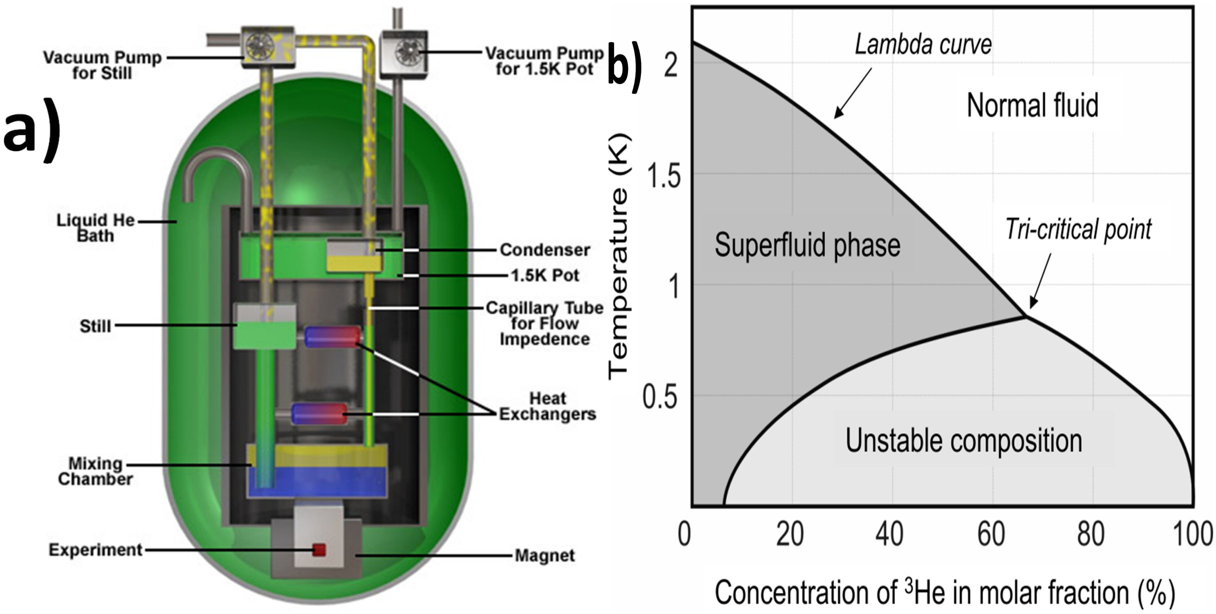

Figure 3.10: a) Schematic diagram of a $^3He/^4He$ dilution refrigerator. Image taken from ref.[39]. b) Phase diagram of $^3He/^4He$ mixtures .

3.5.3 Measurement Set-up

In this work, two different set-ups were used, namely differential conductance and transconductance. Fig. 11 shows the schematic experimental set-up. For the differential conductance measurement a small ac excitation voltage, typically $50\mu V$, was applied between source and drain reservoirs and the conductance through the device was measured using low frequency $(27.3Hz)$ phase-sensitive current detection. In the transcondutance measurement a small ac excitation was applied to the gate electrode and conductance through the device was measured using low frequency phase sensitive detection. All the voltages applied to the device can be swept in small steps via a measurement program called Measkern based on the Linux operating system. This program was developed by the U. Wilhelm at the Max-Planck Institute for Solid State Research in Stuttgart. All our measurements are performed with the Measkern program via GPIB-Bus port interfacing between the experimental instruments and the computer.

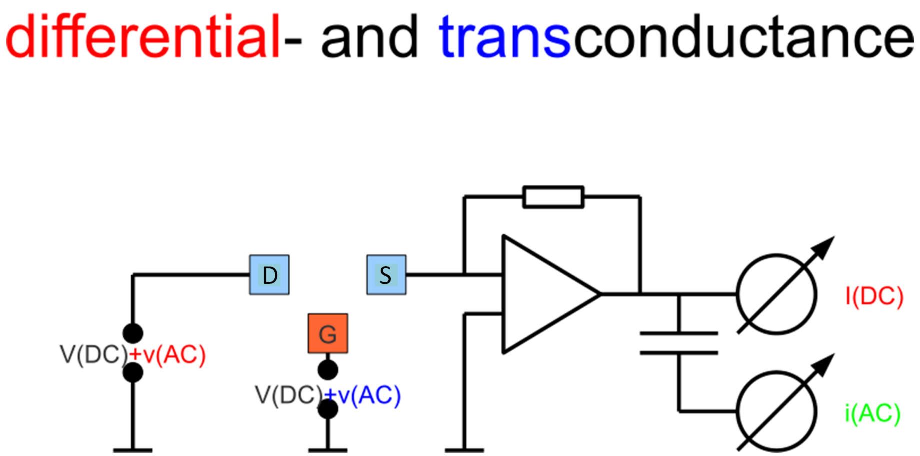

Figure 3.11: Experimental set-up for differential conductance measurement (red) and for transconductance measrement (blue).

Chapter 4

Electron Transport through Single, Double and Triple Quantum Dots

4.1 Introduction

Quantum dots are artificially fabricated devices. The dimensions of such a quantum dot are in the sub-$100nm$ regime. The fermi wavelength of the electrons in the quantum dot is comparable to the dimensions of the quantum dot. In a quantum dot, the electrons occupy a discrete energy spectrum and have a discrete excitation spectrum, analogous to the situation in a real atom. The atomic properties of quantum dots are studied by measuring the current-voltage electron transport properties. Hence, by attaching current and voltage electrodes, the atomic states of the quantum dots can be probed.

If the single quantum dot can be considered an artificial atom, two or three such quantum dots in close vicinity may be considered an artificial molecule. The interaction between these quantum dots may be purely capacitive while a wavefunction overlap may lead to rearrangements as in real molecules.

4.2 Formation of the Quantum Dot

A single top gate device behaves at room temperature like a MOSFET but at low temperature it turns into an SET due to the quantum dot formed below the gate. A quantum dot is formed due to doping modulation along the length of the channel. Here we discuss the formation of a quantum dot in a device with a single top gate. Such devices are useful to study, since they form the foundation of complex designs. Two such devices can be arranged in series or parallel to form a double dot in series or parallel. Fig. 4.1 shows the geometry of a single top gate device with a gate length L, a wire width W and a channel length L_{ch}.

For a device with a single top gate, a wire and source/drain contacts are etched out of a silicon layer of appropriate thickness. Then a polysilicon gate and silicon nitride spacers are formed on the etched silicon nanowire above an SiO_2 gate oxide layer of $5nm$. A heavy implantation is performed to form self-alinged source and drain reservoirs using the gate and spacers as a mask. This protects the region below the gate as well as spacers from heavy implantation, hence it remains undoped. Fig. 4.2a

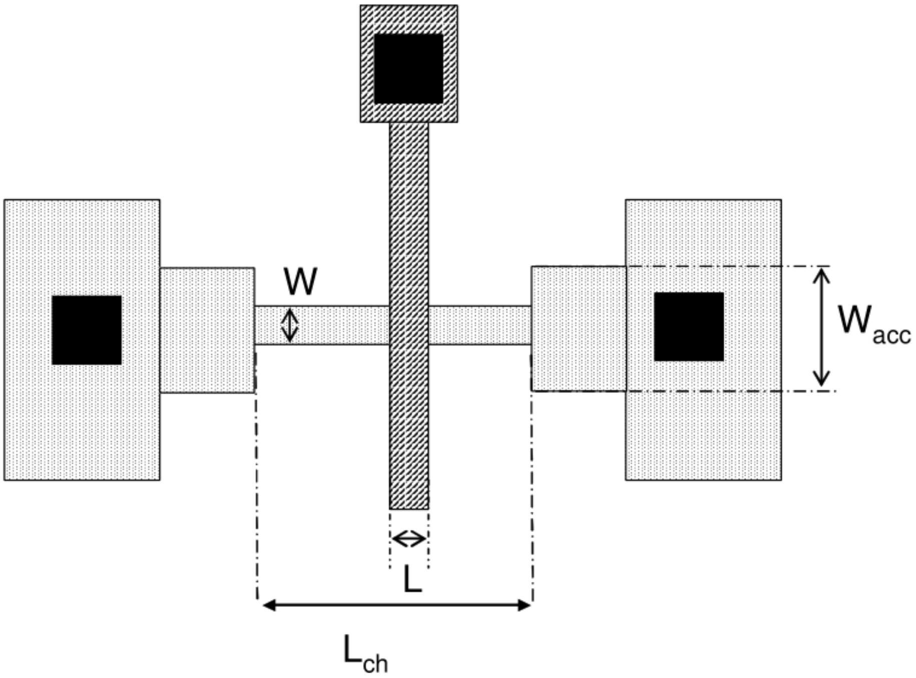

Figure 4.1: Geometry of a single top gate device with gate length L, wire width W and channel length L$_{ch}$.

shows the simulated doping level along the wire for different depths from the top of the wire.

Due to a low doping level below the gate compared to the source and drain regions, the bottom of the conduction band in the source and drain is lower than below the gate. Since source and drain are heavily doped, the bottom of the conduction band edge there is below the Fermi level i.e. these regions are metallic. Fig. 4.2b (bottom) shows the conduction band profile along the length of the wire for increasing gate voltage [40].

Fig. 4.3 shows room temperature measurement of several devices with varying dimensions. The variation of the device turn on (threshold voltage) with changing gate lengths and wire widths can be seen from fig. 4.3. The threshold voltage V_{th} at room temperature for each device was extracted for $I_d = 10^{-7}\frac{W}{L}A$, where I_d is the drain current. For all the devices with single gate measured, the threshold voltage was negative, varying between $-0.1V$ to $-0.4V$.

The nomenclature of the devices in fig. 4.3 is explained in table 4.1 along with the relevant dimensions.

In an n-channel MOSFET at room temperature and at low bias, the potential in the channel is controlled by the gate voltage. For a sufficiently long gate, the electrons cannot tunnel through the barrier. At room temperature, transport is activated thermally. The low bias conductance can therefore be described by [40]:

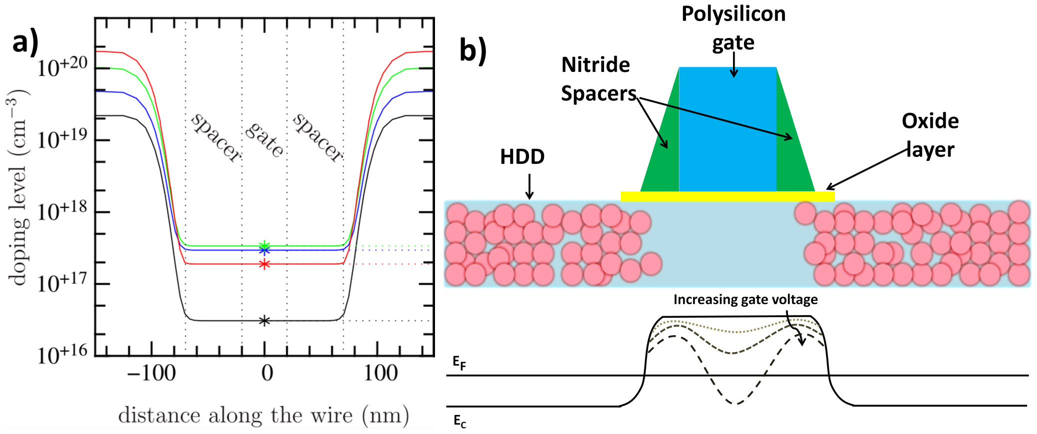

Figure 4.2: a) Simulated doping level along the wire at $1nm$ (black), $5nm$ (blue), $10nm$ (green)and $15nm$ (red) from the top of the film [40]. b) Top: Schematic of the device. Bottom: The conduction band profile for increasing gate voltage is shown schematically which demonstrates the formation of an island separated from source and drain by tunnel barriers.

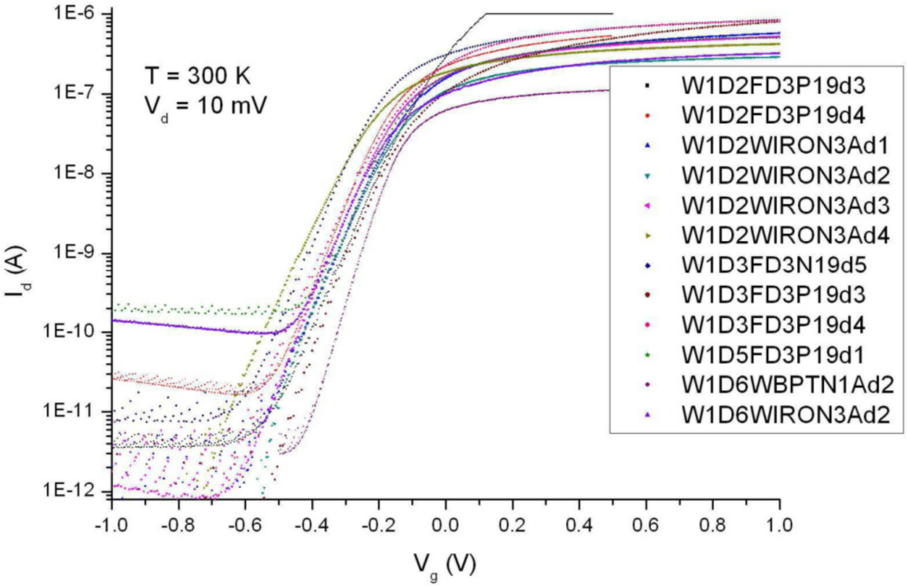

Figure 4.3: Room temperature $I_d - V_g$ characteristics of undoped single gate devices with $40nm$ spacers. For all the devices measured the threshold voltage lies between $-0.1V$ to $-0.4V$.

Device name	Wire width $W(nm)$	Gate length $L(nm)$
W1D2FD3P19d3	60	80
W1D2FD3P19d34	60	60
W1D2WIRON3Ad1	60	60
W1D2WIRON3Ad2	40	40
W1D2WIRON3Ad3	60	60
W1D2WIRON3Ad4	40	40
W1D3FD3N19d5	20	80
W1D3FD3P19d3	60	80
W1D3FD3P19d1	60	60
W1D3FD3P19d4	60	60
W1D6WIRON3Ad2	40	40
W1D6WBPTN1Ad2	20	60

Table 4.1: Nomenclature and dimensions of the devices considered for fig. 4.3.

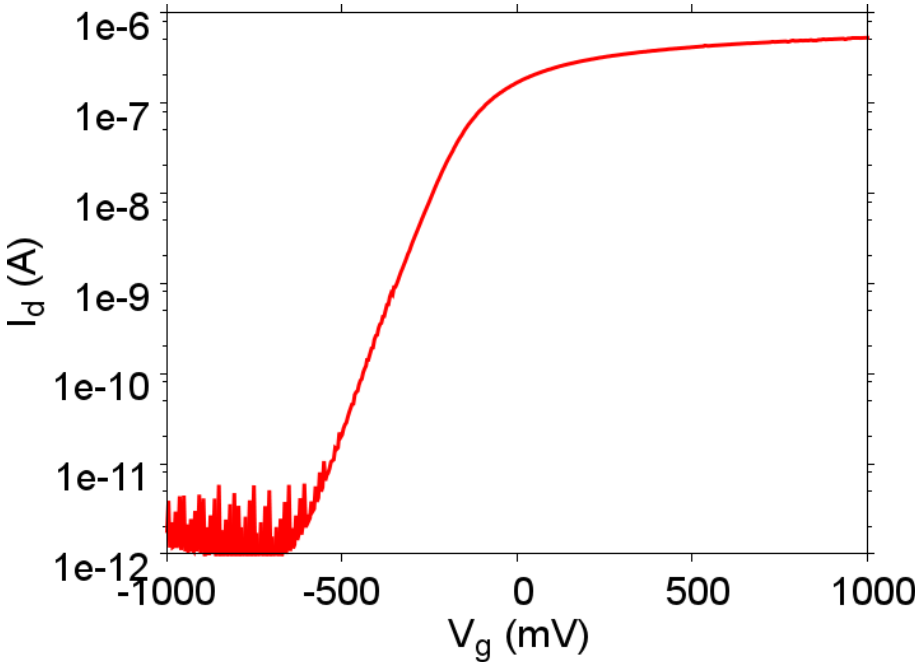

Figure 4.4: Room temperature I_d vs. V_g characteristic at $V_d = 10mV$. Dimensions of the device $L = 60nm$, $W = 60nm$, $T_{Si} = 20nm$.

$$G \sim exp\left(\frac{e\alpha V_g}{k_B T}\right) \tag{4.1}$$

where α is lever arm factor, which describes how well the gate is coupled to the channel. Since α is the ratio of the gate capacitance over the total capacitance, its value is less than 1.

Fig. 4.4 shows on a logarithemic scale the room temperature $I_d - V_g$ of a device with a dimension $L = 60nm$, $W = 60nm$, $T_{Si} = 20nm$. It exhibits a threshold voltage of $V_{th} \approx -88mV$. From fig. 4.4 it can be seen that at low gate voltage ($V_g < V_{th}$) the current increases exponentially, i.e. linearly with gate voltage in our representation. The slope of this linear region is called the subthreshold slope. It is the parameter which tells us how fast the device can be turned ON and OFF. A device characterized by a steeper subthreshold slope shows a faster transition between ON and OFF states of the MOSFET.

As the dimensions of the MOSFET are scaled down, the threshold voltage must also be reduced, since only a limited voltage swing is available to turn the transistor on and off. The $I_d - V_g$ characteristic shown for the device in fig. 4.4 exhibits a subthreshold slope of approx. $100mV/dec$. This value is higher than the average subthreshold slope value of the MOSFET, which is $70mV/dec$.

In the bulk MOSFET, the lever arm factor α is affected by the depletion capacitance coupling the channel to the substrate, but in an SOI transistor this capacitance does not exist. Since the buried oxide is much thicker than the gate oxide, the substrate coupling to the channel is negligible. Therefore, the only loss of gate control is due to the electrostatic coupling to source and drain. This is one of the short channel effects which affect the performance of small transistors.

As the gate voltage is swept from negative to positive voltage, it moves the conduction band edge down and at a particular value, called the threshold voltage; the conduction band edge reaches the Fermi level and the density of states at Fermi level increases abruptly. If we consider the Metal Oxide Semiconductor (MOS) stack as a parallel plate capacitor, the number of carriers increases linearly with gate voltage. In this linear region, the conductance is given by [40][41]:

$$G = \frac{\mu_n C_g (V_g - V_{th})}{L_{ch}^2} \tag{4.2}$$

where C_g is the gate capacitance and μ_n is the electron mobility.

This linear increase in current holds for a small range of V_g. Soon the current curve as a function of gate voltage begins to bend and saturates. The maximum current through the device is limited by the series resistance.

The other short channel effect seen in the above $I_d - V_g$ measurement is a negative threshold voltage. This can be explained as follows: the inversion layer at the oxide-channel is formed at the threshold voltage V_{th}. Electric field lines generated by the charges at metal-oxide interface end on the charges at the oxide-channel interface. But in a short channel, some electric field lines originating from source and drain terminate on the charges in the channel. Thus, the gate voltage required to form the inversion layer is less. All of the samples measured in this work showed a negative threshold voltage.

Devices which worked at room temperature also worked at low temperature unless they were damaged due to improper handling or accidental application of large voltages. In this section, the measurements presented are performed at $4.2K$ in a helium bath. At room temperature the thermal energy available for electrons is approximately $26meV$. Hence, at room temperature electrons can overcome the barrrier formed due to doping modulation. At $4.2K$, the thermal energy available for electrons is $0.36meV$ which is not sufficient to overcome the potential barrier. It is possible to lower the potential barrier by applying positive voltage on the gate. When positive voltage is applied on the gate, the region below the gate forms a quantum dot whereas the region below the spacers forms barriers between the dot and the adjacent source and drain. When gate voltage is increased, the electrochemical potential in the quantum dot is lowered. When the electrochemical potential in the dot lines up with the electrochemical potential in the source and drain, an electron tunnels from the source onto the dot and from the dot out into the drain. This gives rise to a series of conductance oscillations known as Coulomb oscillations.

Fig. 4.5 shows a conductance measurement as a function of gate voltage in the linear regime of a device. Clear Coulomb oscillations are visible. Periodic Coulomb oscillations indicate that the gate capacitance and hence the size of the dot does not

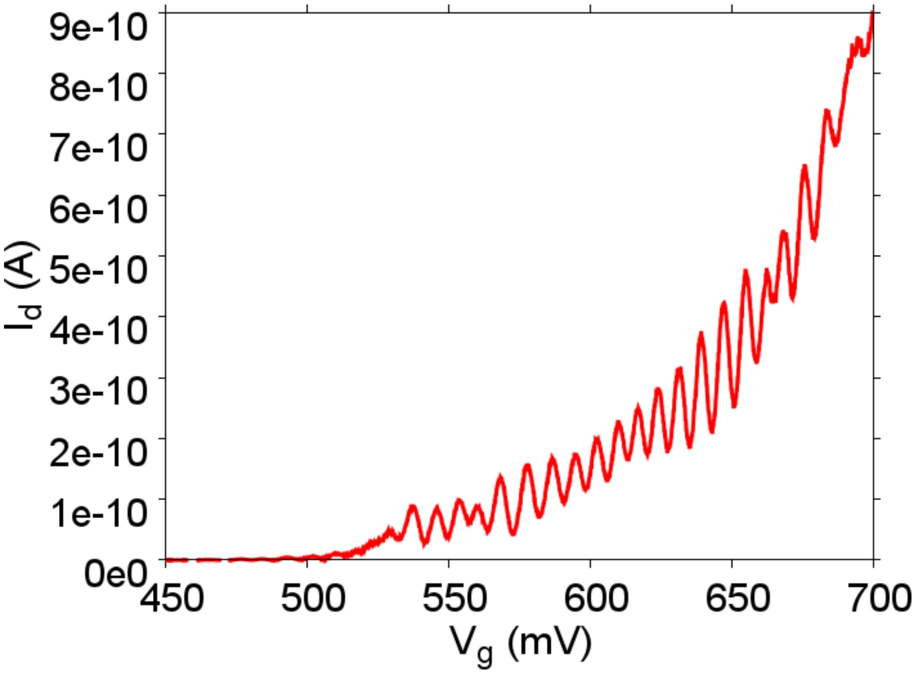

Figure 4.5: $I_d - V_g$ characteristic of single gate MOSFET at $4.2K$ with $V_d = 1mV$ and dimensions $W = 60nm$ and $L = 60nm$.

change over the range of gate voltage shown, i.e. the device is operating in a metallic regime. The period of oscillation is $7.7mV$, which corresponds to a gate capacitance of $\sim 21aF$. Comparing the room temperature threshold with the low temperature threshold (gate voltage at which the first oscillation is observed) of this device, shows that $V_{th} \sim 480mV$ at low temperature and $V_{th} \sim -220mV$ at room temperature (fig. 4.4 and fig. 4.5). For all the devices measured in this work, the threshold voltage at low temperature is higher than the threshold voltage at room temperature. One reason for this shift is that at room temperature, the thermal energy available for electrons is sufficient to overcome the barrier, but at low temperature, electrons cannot overcome this barrier. Hence, at low temperature, the only possible way for an electron to flow through the device is via resonant tunneling. In order for the electrochemical potential of the dot to align with the electrochemical potential of the source and drain (in the linear response limit), a positive voltage must be applied to the gate. Hence, the threshold voltage at low temperature is shifted to a higher gate voltage compared to that at room temperature.

Fig. 4.6a shows the linear response of a device with the dimensions $L = 40nm$, $W = 40nm$, $t_{spacers} = 25nm$ and $T_{Si} = 8nm$ at $4.2K$. In contrast to the linear response of the device in fig. 4.5, which operates in the metallic regime, Coulomb oscillations in fig. 4.6a are aperiodic (see chapter 2 section 2.6), which is essentially a feature of a quantum dot resulting from the finite spacing between the energy levels of the quantum dot. The separation between the first and second oscillation is $\sim 114mV$ (the gate voltage axis can be converted into energy scale by multiplying with the lever arm paremeter, α), which is the sum of the charging energy$\left(\frac{e^2}{C_\Sigma}\right)$ and the energy level separation (ΔE) in the quantum dot, also know as the addition energy. Fig. 4.6b shows the conductance measurement in the non-linear regime at $4.2K$. In the non-linear measurement, Coulomb diamonds are clearly visible. The charging energy for

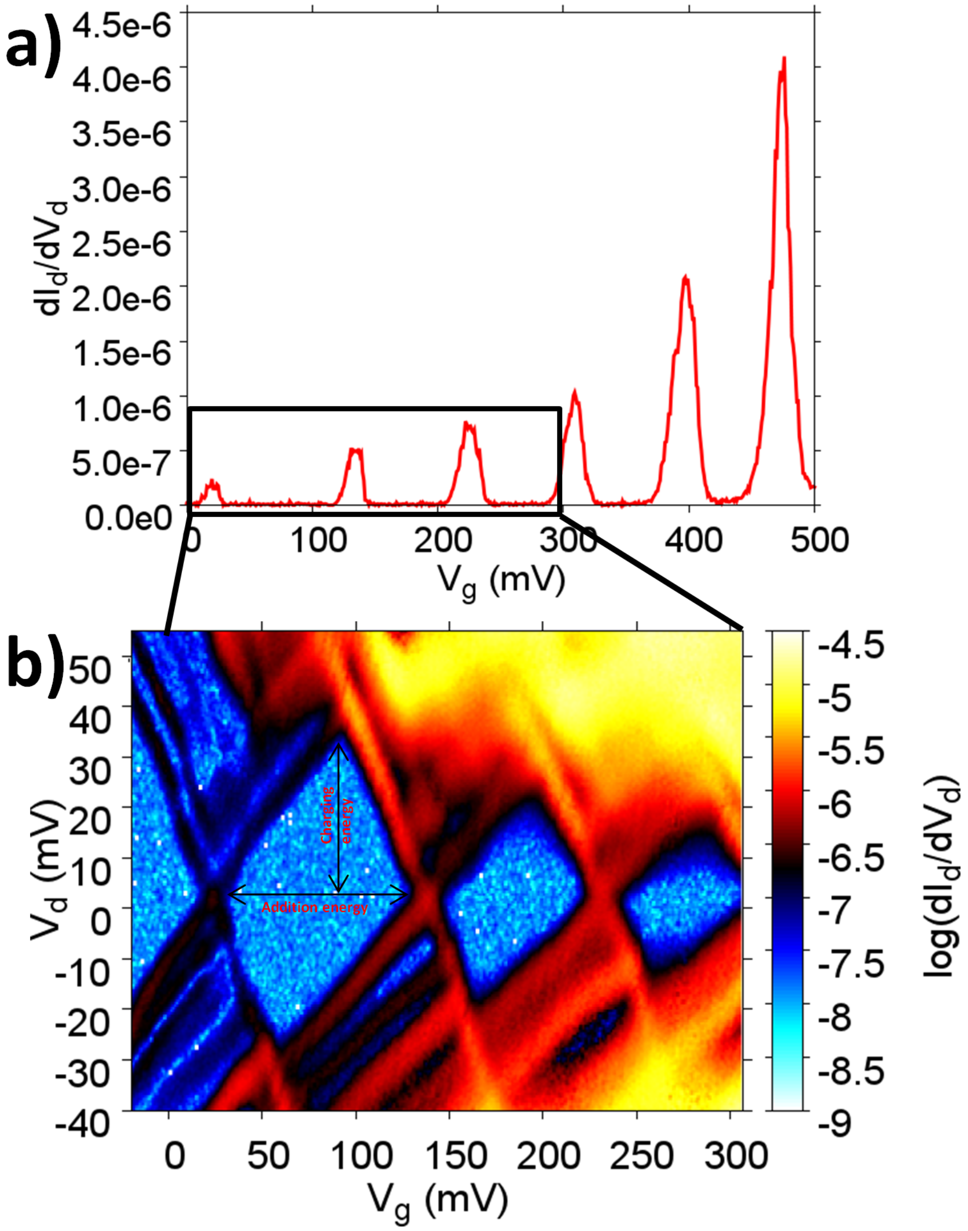

Figure 4.6: a) Linear response of a device with dimensions $L = 40nm$, $W = 40nm$, $t_{spacers} = 25nm$ and $T_{Si} = 8nm$ at $4.2K$. Coulomb blockade oscillations with aperiodic spacing is seen. b) Non-linear response at $4.2K$ showing Coulomb blockade diamonds. In addition to Coulomb blockade diamonds, several excited states are also visible.

the first Coulomb diamond is $\sim 30meV$ (see fig. 4.6b). In addition, a set of lines are running along the edge of the Coulomb diamond, similar to a Coulomb diamond with excited states, as discussed in chapter 2 (section 2.6 (fig. 2.8)). The number of electrons in the Coulomb blockade region is quantized. For a Coulomb diamond with n electrons on the dot, the lines running along the edges of the diamond indicate the energy of the excited states of the $n+1$ electron system. Similarly, the excited states of the n electron system are indicated by the lines running along the edge of the n–1 Coulomb diamond. In the Coulomb diamond shown in fig. 4.6, the conductance lines running along the positive slope edges are more prominently visible compared to the ones with negative slopes. This may be due to asymmetric tunnel barriers. Lines running along the positive slope edges are visible since the conductance through the source-quantum dot barrier is higher than the conductance through the drain-quantum dot barrier. Fig. 4.7 shows the simulated Coulomb diamond for a quantum dot with asymmetric barrier conductance. In fig. 4.7a, the barrier conductance between the drain and the quantum dot is assumed much higher than between the source and the quantum dot. In such a configuration, when an electron jumps on the quantum dot from the source, it immediately escapes into the drain. Since the source-dot barrier is less conducting, most of the voltage drop is across the source-dot barrier and the conductance through the device is dominated by conductance through the source-dot barrier. This results in higher conductance through the lines with a negative slope. Fig. 4.7b shows a simulated Coulomb diamond where the tunnel barrier between the source and the quantum dot is more transparent, which results in higher conductance through the lines with positive slope.

In fig. 4.6, the ground state of Coulomb diamond, i.e. the edge of the Coulomb diamond with positive slope, does not run parallel to the first excited state. Similarly, the negative slope of Coulomb diamonds edge with n electrons and with $n+1$ electrons are not parallel as well. This could be due to a change in size of the quantum dot. With the devices studied in this work, the gate also has control over the barriers. With increasing gate voltage, the barriers between the quantum dot and source and drain are lowered and this change in shape changes the size of the quantum dot. Since the slopes of the Coulomb diamond are associated with the capacitive coupling between the quantum dot and the source, the drain and the gate electrode, a change in size of the dot results in a change of the Coulomb diamond slopes.

Fig. 4.8a shows conductance measurement in the linear regime and fig. 4.8b shows the non-linear response of a device with dimensions $L = 20nm$, $W = 60nm$, $t_{spacer} = 15nm$ and $T_{si} = 12nm$ at $4.2K$. The linear response shows sharp Coulomb peaks with a peak separation of approximately$115mV$. In the non-linear response clear Coulomb diamonds are visible. The charging energy of the first Coulomb diamond is approx. $40meV$. This charging energy suggests that such devices could work at temperatures well beyond $4.2K$ which is one of the important aims of this project and could be useful for future room temprature single electron device applications.

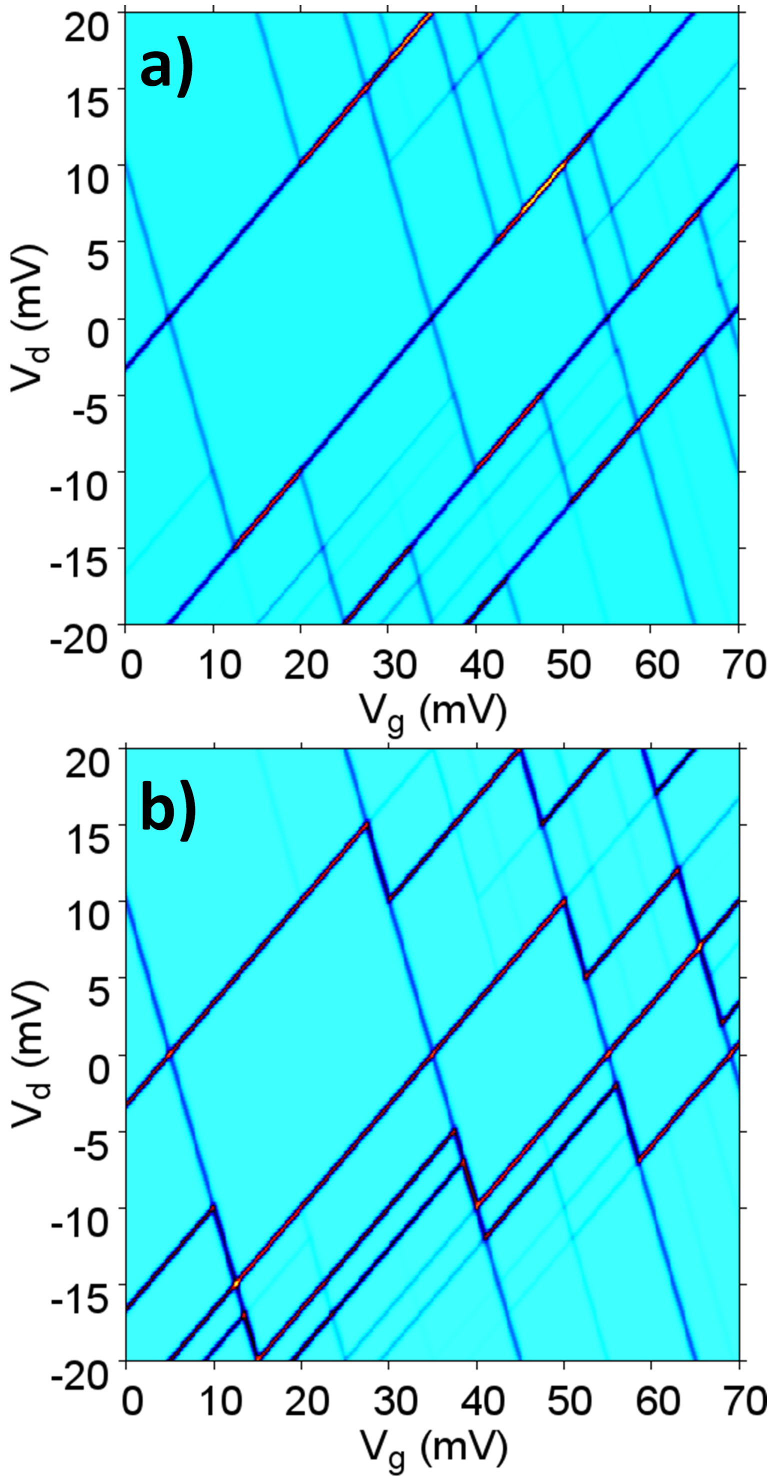

Figure 4.7: a) Simulated Coulomb diamond for a quantum dot with a much higher conductance between the drain and the quantum dot than between the source and the dot, which results in higher conductance through the excited states with negative slope. b) Simulated Coulomb diamond for a quantum dot with a much higher conductance between source and quantum dot than between the drain and the dot, which results in higher conductance through the excited states with positive slope.

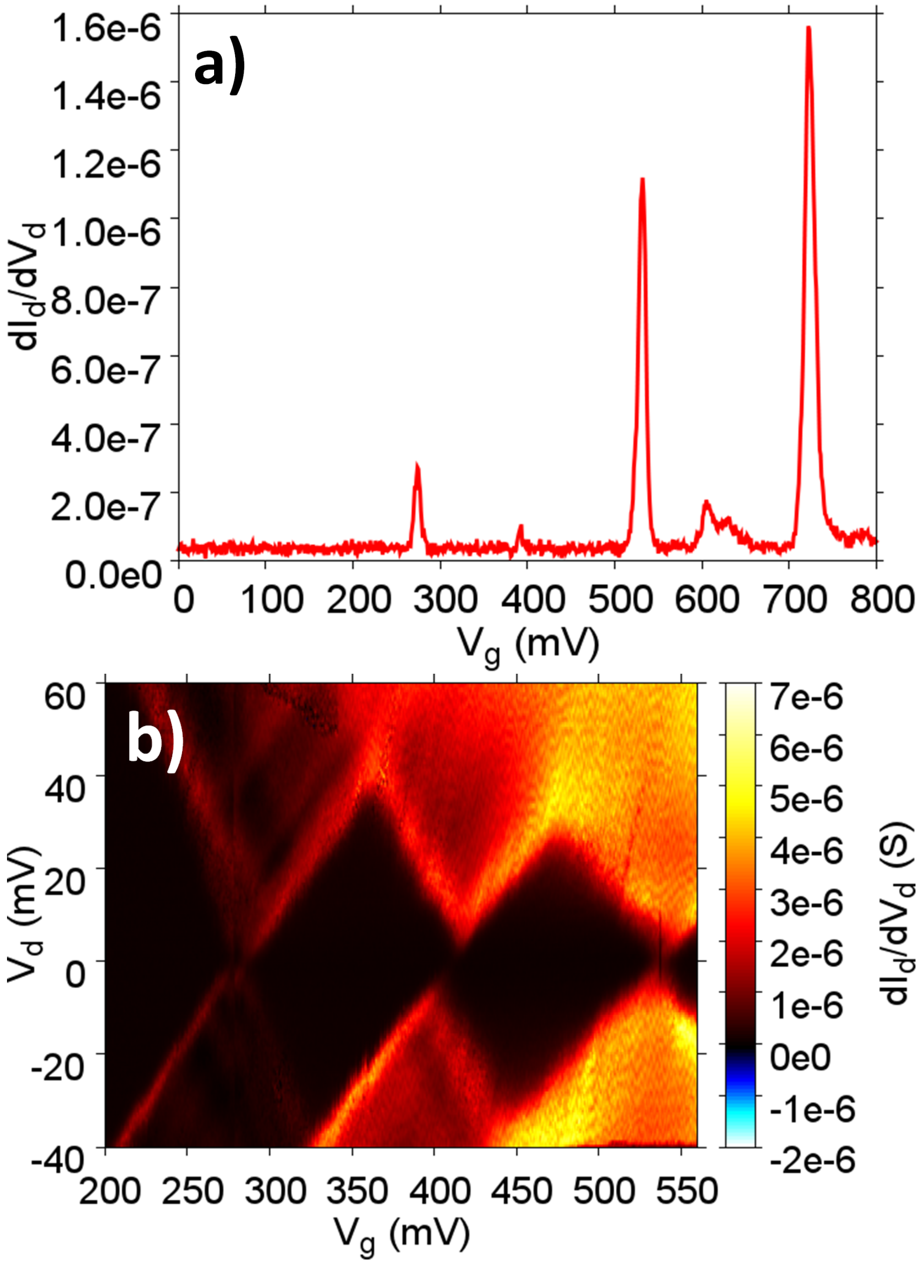

Figure 4.8: a) Linear response of a device with dimensions $L = 20nm$, $W = 60nm$, $t_{spacer} = 15nm$ and $T_{si} = 12nm$ at $4.2K$. Clear Coulomb blockade oscillations are visible. b) Non-linear response at $4.2K$ showing Coulomb blockade diamonds with a charging energy of approxiamtely $40meV$.

4.3 Electron Transport through Double Quantum Dots in Series

In the previous section we studied devices with a single quantum dot. The next step would be to study a system with more than one quantum dot. If a single quantum dot can be considered as an artificial atom, two quantum dots can be considered as an artificial molecule. In analogous manner to a molecule, these two quantum dots can interact with different coupling strength to form an artificial molecule. The two quantum dots can couple weakly (weak tunnel coupling) in order to form an ionic bond where electrons are localized on individual dots or they can couple strongly (strong tunnel coupling) to form a covalent bond where electrons are shared between the dots.

4.3.1 Charge Stability Diagram of a Double Dot in series

The charge stability diagram describes the equilibrium charge states of the double dot in series. In this section, we describe a purely electrostatic model [42][43] in which the influence of the quantum states of the dot is not taken into account. We follow the theoretical description in the ref. [44].

Fig. 4.9 shows the electrostatic model of the double dot in series. The double dot system can be considered as a network of capacitors and resistors with dot $D1$ having n_1 and dot $D2$ having n_2 number of electrons. The tunnel junctions are modelled as a resistor and capacitor in parallel. Gate $G1$ is coupled capacitively to $D1$ via capacitor C_{g1}, whereas gate $G2$ is coupled capacitively to $D2$ via capacitor C_{g2}. For simplicity, the cross capacitance C_{g12} between $G1$ and $D2$ and C_{g21} between $G2$ and $D1$, stray capacitances and the capacitance from the other voltage sources are assumed negligible. $D1$ and source, $D2$ and drain and $D1$ and $D2$ are coupled via a tunnel barriers represented by an RC circuit of resistance R_1, R_2 and R_m and capacitance C_1, C_2 and C_m, respectively. In this section, the linear response will be considered in the limit $V_d \sim 0V$ where the source is grounded and a voltage is applied to the drain.

The total charge Q_{tot1} on the dot $D1$ can be written as the sum of all the charges on the capacitors connected to D_1.

$$Q_{tot1} = C_1(V_1 - V_s) + C_{g1}(V_1 - V_{g1}) + C_m(V_1 - V_2) \tag{4.3}$$

where V_1 and V_2 are the electrostatic potential on the dot $D1$ and $D2$, respectively.

Similarly, the total charge Q_{tot2} on the dot $D2$ can be written as:

$$Q_{tot2} = C_2(V_2 - V_d) + C_{g2}(V_2 - V_{g2}) + C_m(V_2 - V_1) \tag{4.4}$$

The two equations above can be written in a matrix form:

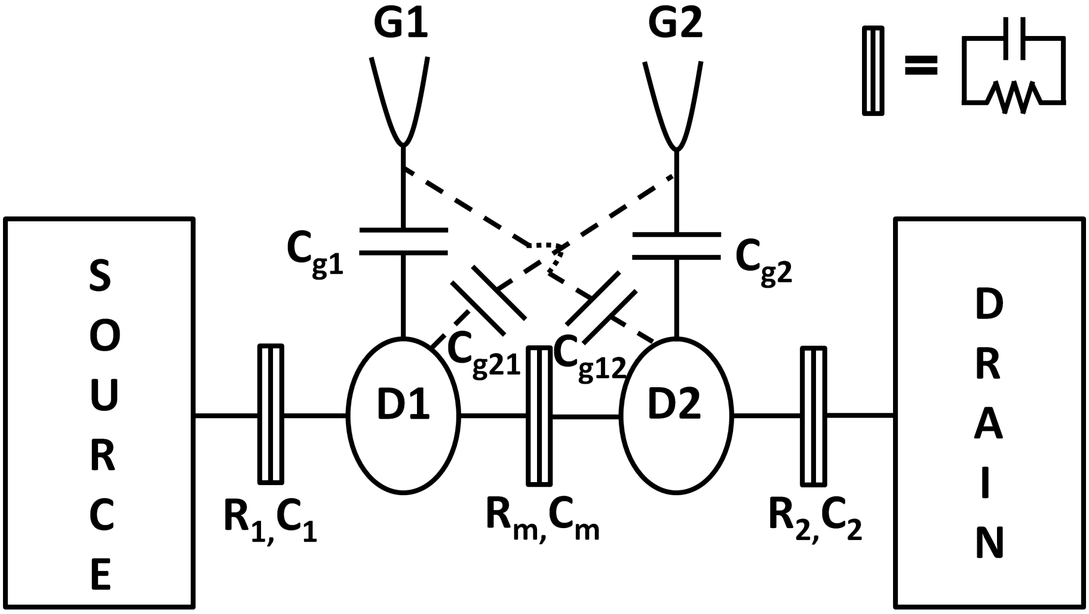

Figure 4.9: Electrostatic model of double dot system. The tunnel barriers are represented as resistors and capacitors in parallel as shown in the inset. The cross capacitance C_{g21} and C_{g12} are shown with dotted lines since they are assumed to be negligible in this section and will be considered later.

$$\begin{pmatrix} Q_{tot1} + C_1 V_s + C_{g1} V_{g1} \\ Q_{tot2} + C_2 V_d + C_{g2} V_{g2} \end{pmatrix} = \begin{pmatrix} C_{tot1} & -C_m \\ -C_m & C_{tot2} \end{pmatrix} \begin{pmatrix} V_1 \\ V_2 \end{pmatrix} \tag{4.5}$$

where $C_{tot1} = C_1 + C_{g1} + C_m$ and $C_{tot2} = C_2 + C_{g2} + C_m$.

Eq. 4.5 is in the form:

$$\overrightarrow{Q} = \overrightarrow{C}\overrightarrow{V} \tag{4.6}$$

The electrostatic energy of the double dot system is given by:

$$U = \frac{1}{2}\overrightarrow{Q}.C^{-1}\overrightarrow{Q} \tag{4.7}$$

Substituting eq. 4.5 in the above eq. 4.7, $Q_{tot1(2)} = -n_{1(2)}e$ and $V_s \approx V_d \approx 0$ for the case of linear response, eq. 4.7 becomes:

$$U(n_1, n_2) = \frac{1}{2} n_1^2 E_{tot1} + \frac{1}{2} n_2^2 E_{tot2} + n_1 n_2 E_m + f(V_{g1}, V_{g2}) \tag{4.8}$$

where

$$\begin{aligned} f(V_{g1}, V_{g2}) \quad &= \quad -\frac{1}{e}\left\{C_{g1}V_{g1}(n_1E_{tot1} + n_2E_m) + C_{g2}V_{g2}(n_1E_m + n_2E_{tot2})\right\} \\ &+ \frac{1}{e^2}\left\{\frac{1}{2}C_{g1}^2V_{g1}^2E_{tot1} + \frac{1}{2}C_{g2}^2V_{g2}^2E_{tot2} + C_{g1}V_{g1}C_{g2}V_{g2}E_m\right\} \end{aligned}$$

and

$$E_{tot1} = \frac{e^2}{C_{tot1}}\left(\frac{1}{\left(1-\frac{C_m^2}{C_{tot1}C_{tot2}}\right)}\right);$$

$$E_{tot2} = \frac{e^2}{C_{tot2}}\left(\frac{1}{\left(1-\frac{C_m^2}{C_{tot1}C_{tot2}}\right)}\right);$$

$$E_m = \frac{e^2}{C_m}\left(\frac{1}{\left(\frac{C_{tot1}C_{tot2}}{C_m^2}-1\right)}\right)$$

$E_{tot1(2)}$is the total charging energy of the dots $D_{1(2)}$ including the interdot coupling term C_m, and E_m is the interdot coupling energy which can be defined as the change in the energy of one dot when an electron is added to the other dot. If the interdot coupling is negligible, i.e. $C_m = 0$, the interdot charging energy is $E_m = 0$. Substituting $C_m = 0$ in the total charging energy expression gives $E_{tot1(2)} = \frac{e^2}{C_{tot1(2)}}$, the charging energy of isolated dots. Hence, substituting $E_m = 0$ in the eq. 4.8 gives the total electrostatic energy of the double dot system as:

$$U\left(n_1,n_2\right) = \frac{\left(-n_1e+C_{g1}V_{g1}\right)^2}{2C_{tot1}} + \frac{\left(-n_2e+C_{g2}V_{g2}\right)^2}{2C_{tot2}} \tag{4.9}$$

This is the sum of electrostatic energies of two isolated dots. If C_m is the dominant capacitance $\left(\frac{C_m}{C_{tot1(2)}} \to 1\right)$, the electrostatic energy is given by:

$$U\left(n_1,n_2\right) = \frac{\left[-\left(n_1+n_2\right)e+C_{g1}V_{g1}+C_{g2}V_{g2}\right]^2}{2\left(\widetilde{C}_1+\widetilde{C}_2\right)} \tag{4.10}$$

Eq. 4.10 is the total electrostatic energy of a single dot with a total charge (n_1+n_2) on it and a total capacitance of $(\widetilde{C}_{tot1}+\widetilde{C}_{tot2})$, where $\widetilde{C}_{tot1(2)} = C_{tot1(2)} - C_m$ is the capacitance of dot $D1(2)$ to the outside world. Thus, a very large interdot capacitance C_m effectively leads to the formation of one big single dot.

The electrochemical potential $\mu_{1(2)}\left(n_1,n_2\right)$ of dot $D1(2)$ is defined as the energy needed to add the $n_{1(2)}th$ electron to the dot $D1(2)$, while $D2(1)$ is occupied by $n_{2(1)}$ electrons. Using the expression for the total electrostatic energy in eq. 4.8, the electrochemical potentials of the two dots are given by:

$$\mu_1\left(n_1,n_2\right) := U\left(n_1,n_2\right) - U\left(n_1-1,n_2\right)$$

$$\mu_1\left(n_1,n_2\right) = (n_1-\frac{1}{2})E_{tot1} + n_2E_m - \frac{1}{e}\left(C_{g1}V_{g1}E_{tot1}+C_{g2}V_{g2}E_m\right) \tag{4.11}$$

$$\mu_2(n_1,n_2) := U(n_1,n_2) - U(n_1,n_2-1)$$

$$\mu_2(n_1,n_2) = (n_2 - \frac{1}{2})E_{tot2} + n_1 E_m - \frac{1}{e}\left(C_{g2}V_{g2}E_{tot2} + C_{g1}V_{g1}E_m\right) \tag{4.12}$$

The addition energy of dot $D1$ is defined as the change in the electrochemical potential $\mu_1(n_1,n_2)$ of dot $D1$ when the electron number on $D1$ changes by one for a given set of gate voltages. In the classical regime this energy is equal to the charging energy of the dot $D1$. The addition energy of dot $D1$ is given by:

$$\mu_1(n_1+1,n_2) - \mu_1(n_1,n_2) = E_{tot1}$$

Similarly, the addition energy of dot $D2$ equals E_{tot2} and is given by:

$$\mu_2(n_1,n_2+1) - \mu_2(n_1,n_2) = E_{tot2}$$

and the interdot charging energy is given by:

$$\mu_1(n_1,n_2+1) - \mu_1(n_1,n_2) = \mu_2(n_1+1,n_2) - \mu_1(n_1,n_2) = E_m.$$

Eq. 4.11 and eq. 4.12 enable a charge stability diagram to be defined. This charge stability diagram gives the equilibrium number of electrons n_1 on dot $D1$ and n_2 on dot $D2$ as a function of gate voltages V_{g1} and V_{g2}. In the linear regime, $V_d = 0$ and hence $\mu_s = \mu_d = 0$. Hence, the equilibrium charge on the dots for a given combination of gate voltages V_{g1} and V_{g2}, are the largest allowed values of n_1 and n_2 for which both $\mu_1(n_1,n_2)$ and $\mu_2(n_1,n_2)$ are less than zero. If either $\mu_1(n_1,n_2)$ or $\mu_2(n_1,n_2)$ is greater than zero, the electron escapes to the lead. This restriction with the condition that n_1 and n_2 must be an integer, creates a hexagonal domain in the $V_{g1} - V_{g2}$ space in which the charge configuration is stable.

For a very weak interdot coupling $(C_m = 0)$ between the dots $D1$ and $D2$ the charge stability looks as shown in fig. 4.10a, where each gate voltage $V_{g1(2)}$ is changing the charge on $D_{1(2)}$without affecting the charge on the other dot. This leads to a square charge stability diagram. When C_m is non-zero, the charging of one of the dots by an additional single electron changes the electrostatic energy of the other dot, and this effectively causes a shift of the electrochemical potential in the region where the electrochemical potential of both dots intersect. This results in a hexagonal domain as shown in fig. 4.10b. The vertices of the square domains develop into 'triple-points'. When C_m becomes the dominant capacitance $(C_m/C_{tot1(2)} \rightarrow 1)$, the triple-point separates and reaches its maximum (see fig. 4.10c). The double dot behaves like one single big dot with charge $(n_1 + n_2)$ on it, as seen from eq. 4.10.

We are now consider transport through the double dot in series in the linear regime, implying $\mu_s - \mu_d = -eV \approx 0$. In order to measure current through the device, the tunnel

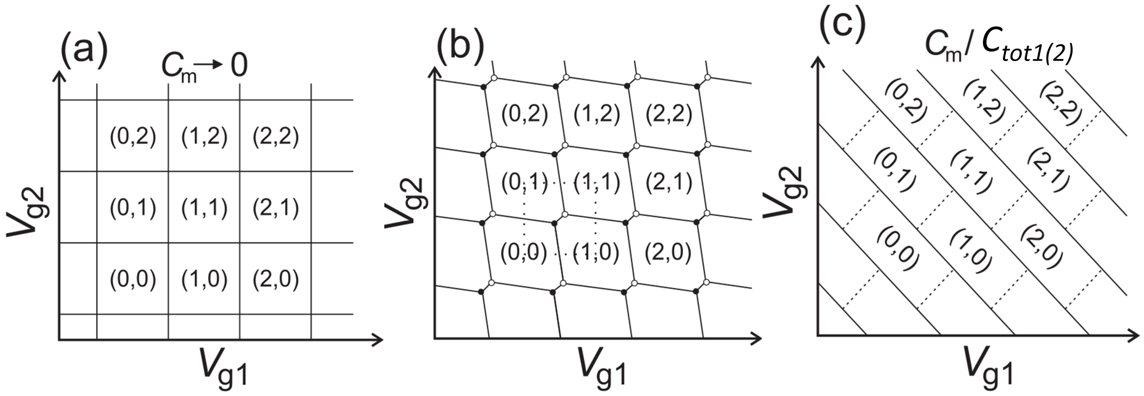

Figure 4.10: Charge stability of double dot system in different regime. a) In the limit $C_m = 0$ (weak interdot coupling) b) Intermediate coupling which results in honeycomb domain c) In the limit $C_m \to C_{1(2)}$ where the system behaves as a single dot with $n_1 + n_2$ electrons. Image taken from ref. [44].

barriers should be transparent enough to allow electron exchange between the dots and dot and reservoirs, at the same time, the tunnel barriers should also be opaque enough to ensure a quantized number of electrons on each dot. A conductance resonance is seen in double dot in series when electrons tunnel through both the dots. This condition is satisfied when the three charge states in the honeycomb diagram meet in a single point. In fig. 4.10b, we can distinguish two types of triple points :(•) and (○). Each type of triple point corresponds to a different charge transfer process. At the triple point (•), an electron is pushed through the double dot which cycles the system through the sequence $(n_1,n_2) \to (n_1+1,n_2) \to (n_1,n_2+1) \to (n_1,n_2)$. This process is demonstrated by the counter clockwise path e in fig. 4.11a and an electron tunnels from the source to the drain sequentially. At the other triple-point (○), an hole is pushed through the double dot which cycles the system through the sequence

$$(n_1+1,n_2+1) \to (n_1+1,n_2) \to (n_1,n_2+1) \to (n_1+1,n_2+1),$$

and corresponds to the clockwise path h in fig. 4.11a. This can be interpreted as the sequential tunneling of a hole in the direction opposite to the electron.

The extention of a hexagon in V_{g1} direction can be determined by (c.f. fig. 4.11b):

$$\mu_1\left(n_1,n_2;V_{g1},V_{g2}\right) = \mu_1\left(n_1+1,n_2,V_{g1}+\Delta V_{g1},V_{g2}\right) \tag{4.13}$$

which gives the period of oscillations along V_{g1} using eq. 4.11:

$$\Delta V_{g1} = \frac{e}{C_{g1}} \tag{4.14}$$

and similarly, the period of oscillations along V_{g2} follows from:

$$\mu_2\left(n_1,n_2;V_{g1},V_{g2}\right) = \mu_2\left(n_1,n_2+1,V_{g1},V_{g2}+\Delta V_{g2}\right) \tag{4.15}$$

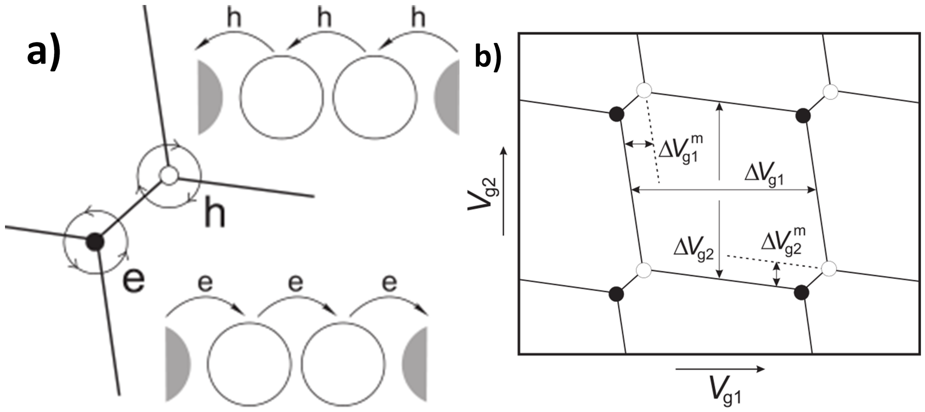

Figure 4.11: a) Transport of electron and hole at the triple point. b) Schematic stability diagram showing the Coulomb peak spacings. These spacings can be determined experimentally by connecting the triple-points. Images taken from ref. [44].

which gives (using eq. 4.12)

$$\Delta V_{g2} = \frac{|e|}{C_{g2}} \tag{4.16}$$

The effect of interdot coupling can be seen from the condition (see fig. 4.11b)

$$\mu_1\left(n_1, n_2; V_{g1}, V_{g2}\right) = \mu_1\left(n_1, n_2 + 1, V_{g1} + \Delta V_{g1}^{m}, V_{g2}\right) \tag{4.17}$$

which yeilds

$$\Delta V_{g1}^{m} = \frac{|e| C_m}{C_{g1} C_{tot2}} = \Delta V_{g1} \frac{C_m}{C_{tot2}} \tag{4.18}$$

and similarly

$$\mu_2\left(n_1, n_2; V_{g1}, V_{g2}\right) = \mu_1\left(n_1 + 1, n_2, V_{g1}, V_{g2} + \Delta V_{g2}^{m}\right) \tag{4.19}$$

gives

$$\Delta V_{g2}^{m} = \frac{|e| C_m}{C_{g2} C_{tot1}} = \Delta V_{g2} \frac{C_m}{C_{tot1}} \tag{4.20}$$

The dimensions of the honeycomb is related to the capacitances of the double dot system as shown in fig.4.11b.

So far, the assumption in the discussion was that the cross capacitances C_{g21} and C_{g12} are negligible when determining the electrostatic energy of the double dot system, as

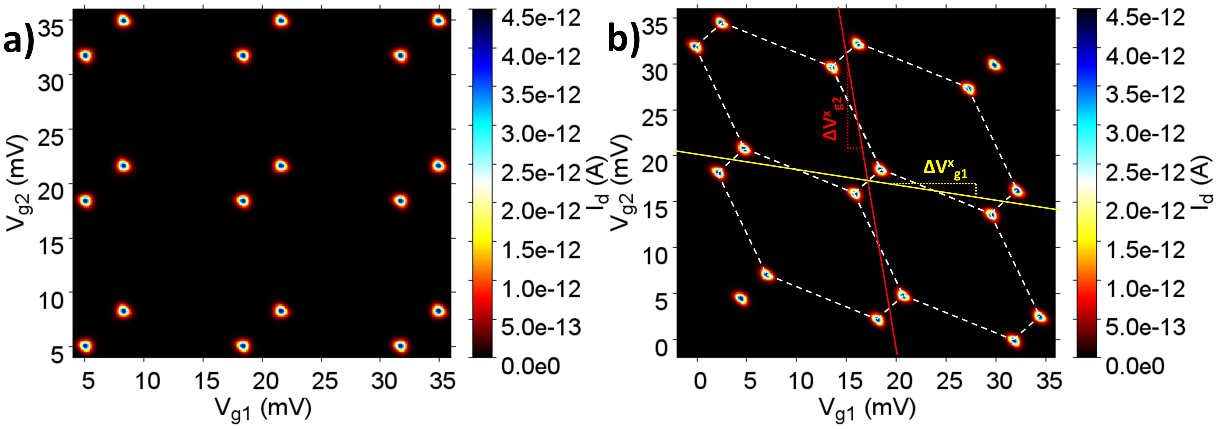

Figure 4.12: a) Simulated honeycomb pattern without taking into acount the cross capacitance between $G1$ and $D2$ and vice versa which results in triple points forming a square lattice parallel to V_{g1} and V_{g2}. b) Simulated honeycomb pattern including the cross capacitance. The honeycomb pattern is tilted with the triple points lying on a line with negative slope along V_{g1} and V_{g2}.

indicated in fig. 4.9 by dotted lines. Measurements on the double dot system have shown that the cross capacitances can be large enough to contribute to the total electrostatic energy and hence they cannot be neglected. In order to take them into account, eq. 4.3 and eq. 4.4 are modified according to

$$\overrightarrow{Q} = \begin{bmatrix} Q_{tot1} + C_{g1}V_{g1} + C_{g21}V_{g2} \\ Q_{tot2} + C_{g2}V_{g2} + C_{g12}V_{g1} \end{bmatrix} \tag{4.21}$$

where $Q_{tot1(2)}$ is the total charge on the dot $D1(2)$ and C_{g21} is the cross capacitance from gate $G2$ to dot $D1$ and C_{g12} is the cross capacitance from gate $G1$ to dot $D2$. Substituting the eq. 4.21 in eq. 4.7, we obtain the electrostatic energy of the double dot system which now also includes the cross capacitance:

$$U = \frac{1}{2}\vec{Q}.C^{-1}\vec{Q}$$

i.e.

$$U = \frac{1}{2}\vec{Q}\begin{pmatrix} C_{\mathrm{tot1}} & -C_m \\ -C_m & C_{\mathrm{tot2}} \end{pmatrix}^{-1}\vec{Q}$$

$$U = \frac{1}{C_{tot1}C_{tot2} - C_m^2}\left(\frac{1}{2}C_{tot1}a^2 + \frac{1}{2}C_{tot2}b^2 + C_m ab\right)$$

where

$$a = \left(-en_2 + C_{g2}V_{g2} + C_{g12}V_{g1}\right)$$

$$b = \left(-en_1 + C_{g1}V_{g1} + C_{g21}V_{g2}\right)$$

where $n_{1(2)}$ is the number of electrons on dot $D1(2)$, $C_{tot1} = C_1 + C_m + C_{g1} + C_{g21}$ is the total capacitance of dot $D1$ and $C_{tot2} = C_2 + C_m + C_{g2} + C_{g12}$ is the total capacitance of dot $D2$.

$$C_{g21} = \frac{e}{|\Delta V_{g2}^x|} \tag{4.22}$$

$$C_{g12} = \frac{e}{|\Delta V_{g1}^x|} \tag{4.23}$$

where $\Delta V_{g1(g2)}^x$ is the value of the gate voltage $V_{g1(g2)}$, determined from the fig. 4.12b. The effect of cross capacitance can be seen in the fig. 4.12b. The honeycomb pattern in fig. 4.12b is tilted in the presence of cross capacitance in compaison to the one in fig. 4.12a. The triple points lie on a line with negative slope. The honeycomb cell is related to the capacitances of the system. Due to the influence of the cross capacitance, the relation given for the gate and the interdot capacitances has to be modified. From the voltage separation in fig. 4.12b the gate capacitance and interdot capacitance can be given as:

$$C_{g2} = \frac{e}{\Delta V_{g2}} - C_{g21}\frac{\Delta V_{g2}^m}{\Delta V_{g2}} \tag{4.24}$$

$$C_{g1} = \frac{e}{\Delta V_{g1}} - C_{g12}\frac{\Delta V_{g1}^m}{\Delta V_{g1}} \tag{4.25}$$

The interdot capacitance can be extracted from the relation in eq. 4.18 and eq. 4.20:

$$C_m = C_{tot1}\frac{\Delta V_{g2}^m}{\Delta V_{g2}} = C_{tot2}\frac{\Delta V_{g1}^m}{\Delta V_{g1}} \tag{4.26}$$

4.3.2 Quantum States

So far the discussion of the charge stability in the double dot system was completely classical. However, due to strong electron confinement within the quantum dot the energy levels in the quantum dot are quantized leading to a discrete energy spectrum. These quantized energies must be taken into account in the electrochemical potential. Therefore, the electrochemical potential for adding an electron in the energy level n of dot i can be defined by $\mu_{i,n}$. Within the constant interaction model, $\mu_{i,n}$ is the sum of the classical electrochemical potential $\mu_i^{classical}$ and the single-particle energy E_n:

$\mu_{i,n} = \mu_i^{classical} + E_n$. Therefore, the energy needed for adding the $(n_1+1)th$ electron on dot $D1$ occupying energy level m in which the energy level n is already occupied by the $n_1 th$ electron, is given by:

$$\mu_{1,m}(n_1+1,n_2) - \mu_{1,n}(n_1-n_2) = E_{tot1} + (E_m - E_n)$$

$$= E_{tot1} + \Delta E \tag{4.27}$$

Similarly, the energy needed to add $(n_2+1)th$ electron on dot $D2$ is given by:

$$\mu_{2,m}(n_1,n_2+1) - \mu_{2,n}(n_1,n_2) = E_{tot2} + \Delta E$$

Note that for a spin degeneracy energy level ΔE can be zero. Due to discrete energy levels in the dot, the dimensions of the honeycomb cell changes from the classical regime as follows:

$$\Delta V_{g1(2)} = \frac{e}{C_{g1(2)}}\left(1 + \frac{\Delta E}{E_{tot1(2)}}\right) \tag{4.28}$$

$$\Delta V^m_{g1(2)} = \frac{eC_m}{C_{g1(2)}C_{tot2(1)}}\left(1 + \frac{\Delta E}{E_m}\right) \tag{4.29}$$

The electronic configuration which gives the lowest possible total energy in dot $D1(2)$ is the ground state whereas any configuration which gives a higher total energy is an excited state of the dot. The electrochemical potential for adding the $n_{1(2)}th$ electron to an unfilled energy level of the $n_{1(2)} - 1th$ electron state is labelled as $\mu_{i,j}(n_1,n_2)$, where i denotes the number of the dot i.e. $i = 1$ denotes dot $D1$ and $i = 2$ denotes dot $D2$ and j denotes the electron states i.e. $j = 0$ denote the ground state and $j = 1,2,3...$ denotes the unfilled excited states.

Fig. 4.13a shows the alignment of the ground state electrochemical potential $\mu_{1,0}(1,0)$ and $\mu_{2,0}(0,1)$ with the electrochemical potentials of the leads within the transport window allowing the electrons to tunnel from left reservoir to the right reservoir. The electron does not tunnel through the double dot system for alignment of arbitary combination of electrochemical potentials in dot $D1$and $D2$, e.g. the alignment of $\mu_{1,0}(1,0)$ and $\mu_{2,0}(1,1)$ does not lead to a current through the double dot. The electron transport takes place through ground states in the linear regime whereas excited states play a role in the non-linear regime.

Fig. 4.13b shows the configuration of the ground state electrochemical potential on some places in the stability diagram. The dashed lines are the extension of the solid lines forming the honeycomb cell. These dashed lines help to find the position of both

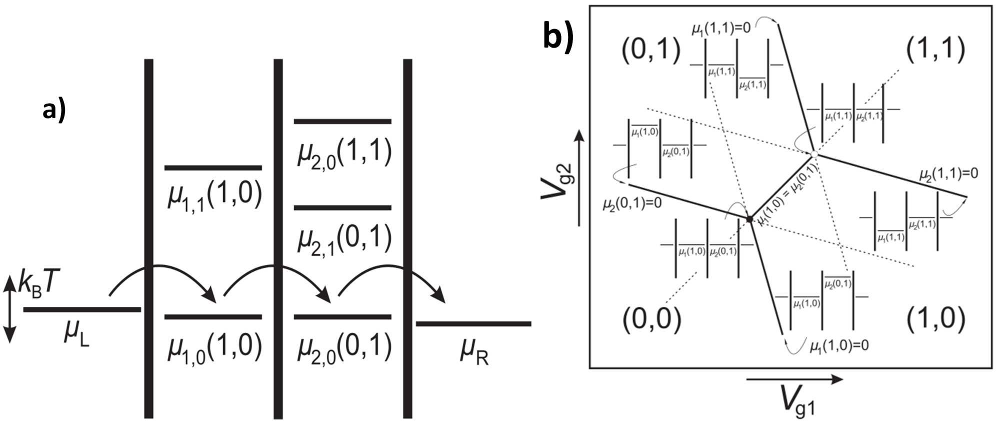

Figure 4.13: a) Schematic diagram of the electrochemical potentials $\mu_{i,n}(n_1,n_2)$ in dots and electrodes in the linear regime. The first subscript i indicates either the electrode source, drain or the dot $D1$ or $D2$. The second subscript n refers to the nature of the dot energy state ($n = 0$ corresponds to the ground state, $n > 0$ to the nth excited state). b) Honeycomb cell of the double-dot stability diagram in the vicinity of triple points. Solid lines are separating four different charge states. At the solid line connecting the two triple points, the charge states $(0,1)$ and $(1,0)$ are degenerate. At the other solid lines the electrochemical potential of at least one dot is zero and thus equals the electrochemical potential of the electrodes. The dashed lines are the extensions of the solid lines within the honeycomb cells. The triple-points lie on the crossing points between the solid lines. The schematic diagrams show the configuration of the ground-state electrochemical potentials on the corresponding place in the honeycomb diagram. Image taken from ref. [44].

the chemical potentials on a certain place. When the dashed lines cross each other e.g. the charge domains $(0,1)$ and $(1,0)$, the two electrochemical potentials align but do not result in a current through the double dot.

4.3.3 Molecular States in Double Quantum Dot

So far we assumed that the coupling between the two dots was completely electrostatic and the quantum mechanical tunneling was neglected. The two dots can form an ionic-like bond if the interdot coupling is weak and the electron wavefunction is localized on either dot. Hence, the electron wavefunction leakage from one dot into the other is minimal. In such a case, quantum states on individual dots are very weakly affected by their interdot coupling. When the interdot coupling increases the two dots form a covalent-like bond and the electron wavefunctions are no longer localized on either dot, resulting in the wavefunction overlap. This results in the formation of collective molecular states that are characteristic of the coupled-dot system forming a symmetric and anti-symmetric state, where the energy separation between these two states is propotional to the tunneling strength between the dots. Due to the electron wavefunction on one dot overlapping the electron wavefunction on the other dot, electron transport takes place even outside the region of triple point depending on the strength of the wavefunction overlap. This makes the honeycomb boundaries rounded as shown in fig. 4.14a [46].

Consider two weakly coupled dots, described by a total Hamiltonian $\mathbf{H_0}$ with eigenstates $|\phi_1>$and $|\phi_2>$ and corresponding energies E_1 and E_2.

$$\mathbf{H_0}|\phi_1>= E_1|\phi_1> \tag{4.30}$$

$$\mathbf{H_0}|\phi_2>= E_2|\phi_2> \tag{4.31}$$

The finite tunnel coupling between the energy levels in both the dots is defined by a non-diagonal tunnel matrix **T**, which can be written as:

$$\mathbf{T} = \begin{pmatrix} 0 & t_{12} \\ t_{21} & 0 \end{pmatrix}, t_{12} = t_{21}^{*}, t_{21} = |t_{21}|e^{i\varphi} \tag{4.32}$$

Including the tunnel matrix **T** in the total Hamiltonian $\mathbf{H_0}$ gives the new Hamiltonian, $\mathbf{H} = \mathbf{H_0} + \mathbf{T}$ with the delocalized eigenstates $|\psi_S>$ and $|\psi_A>$and corresponding eigenenergies E_S and E_A:

$$\mathbf{H}|\psi_S>= E_S|\psi_S>$$

$$\mathbf{H}|\psi_A>= E_A|\psi_A> \tag{4.33}$$

The eigenvalues of eq. 4.33 can be written in terms of eigenvalues of uncoupled double dots and the tunnel matrix elements as follows [45][46]:

$$E_S = E_M - \sqrt{\frac{1}{4}(\Delta E)^2 + |t_{12}|^2}$$

$$E_A = E_M + \sqrt{\frac{1}{4}(\Delta E)^2 + |t_{12}|^2} \tag{4.34}$$

where

$$E_M = \frac{1}{2}(E_1 + E_2)$$

and

$$\Delta E = E_1 - E_2$$

The eigenstates $|\psi_S>$ and $|\psi_A>$ can be written as:

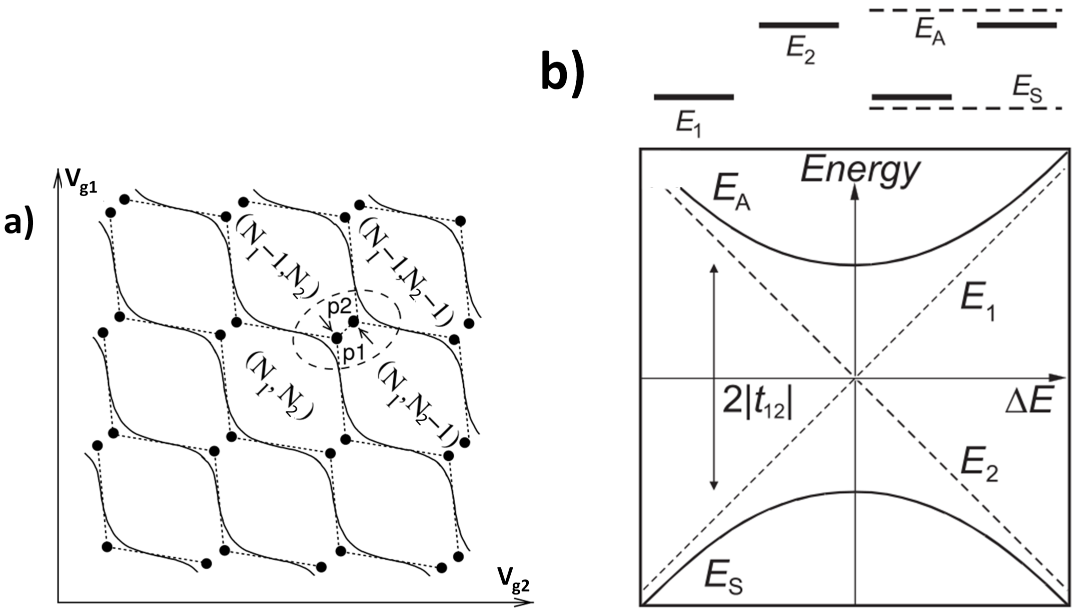

Figure 4.14: a) Charge stability diagram of a strongly tunnel-coupled double dot system which results in rounding of honeycomb boundaries. Image taken from ref. [46]. b) Above: Schematic diagrams of a two-level system. Below: Energies E_S and E_A versus the energy difference $\Delta E = E_1 - E_2$. For very weak tunnel coupling ($|t_{12}| \approx 0$), the levels cross at the origin (dashed straight lines). For finite coupling, an 'anti-crossing' occurs: the curves belonging to E_S and E_A as a function of ΔE are branches of a hyperbola (solid lines) whose asymptotes are the unperturbed levels. Image is taken from ref. [44].

$$|\psi_S> = -\sin\frac{\theta}{2}e^{-i\frac{\varphi}{2}}|\phi_1> + \cos\frac{\theta}{2}e^{i\frac{\varphi}{2}}|\phi_2>$$

$$|\psi_A> = \cos\frac{\theta}{2}e^{-i\frac{\varphi}{2}}|\phi_1> + \sin\frac{\theta}{2}e^{i\frac{\varphi}{2}}|\phi_2> \tag{4.35}$$

Fig. 4.14b shows the eigenenergies of the double dot system as a function of ΔE. Since $\Delta E = E_1 - E_2$, the effect of coupling between the double dot is strongest when both the unperturbed energy levels E_1 and E_2 cross i.e. when $\Delta E = 0$. When ΔE is large, the eigenenergies of the coupled dot system approaches that of the uncoupled dots, E_1 and E_2.

4.4 Measured Stability Diagrams

The device measured to study the double dot configuration is schematically shown in fig. 4.15a. The device has two top gates separated by a distance of $50nm$ which can form two quantum dots in series. By sweeping each gate and holding the other gate at fixed high voltage, each dot can be characterized as a SET. All measurements in this section were done at liquid helium temperature in a helium dewar ($4.2K$) using a differential conductance measurement set-up. Fig. 4.15a shows on the top the schematic of the device and below the conduction band profile for increasing gate voltages is sketched. Changing the gate voltage also changes the barriers between the two dots

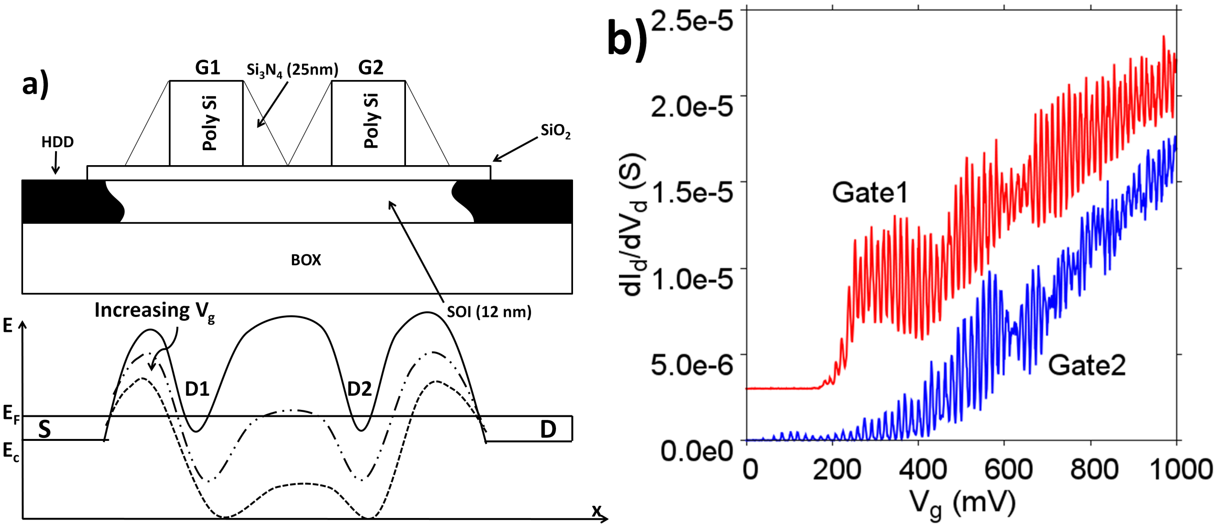

Figure 4.15: a) Top: Schematic of the device. Bottom: the bottom of the conduction band is drawn for various gate voltages. The horizontal line is the Fermi energy fixed by the source and drain. b) linear response at $4.2K$ for each gate holding the other gate at $1V$.

which allows us to study the interaction between them in different coupling regimes varying from weakly coupled to strongly coupled. Fig. 4.15b shows a linear response for $G1$ holding $G2$ at $1V$ and vice versa. The linear response shows a large number of Coulomb oscillations for each gate voltage. The period of Coulomb oscillations for $G1$ is $13.3mV$ and for $G2$ it is $14.3mV$.

The corresponding gate capacitance for $G1$ is $12aF$ and for $G2$ it is $11.2aF$. In the non-linear response (fig. 4.16), for $G2$ clear Coulomb blockade diamonds are visible while holding $G1$ at $1V$. For $G1$, the Coulomb diamonds show sawtooth nature. This is because dot $D2$ is not weakly coupled to the dot $D1$ which gives rise to the sawtooth nature of the Coulomb diamonds [47]. The capacitive coupling between source and dot D1 is approximately $5aF$, whereas the capacitance between drain and dot D2 is approximately $4.5aF$. These values are extracted from fig. 4.17a and fig 4.17b.

To study the interaction between the two dots, $G1$ and $G2$ were swept in different voltage ranges. When the gate voltage is swept, it changes the electrochemical potential of the dot formed below that gate, in addition it also lowers the barriers. So with changing gate voltage the interdot capacitance also changes. For low gate voltages the interdot capacitance between dot $D1$ and dot $D2$ is small and hence the effect of charging dot $D1$ is very weakly seen by dot $D2$ and vice-versa. Similarly, the effect of sweeping $G2$ is weakly seen by dot $D1$ and vice-versa. Therefore, the gate voltage V_{g1} essentially changes the charge on dot $D1$ without affecting the charge on dot $D2$ and the gate voltage V_{g2} changes the charge on dot $D2$ without affecting the charge on dot $D1$. This results in a rectangular conductance pattern as shown in fig. 4.17a. Vertical and horizontal charging along V_{g2} and V_{g1} respectively, indicates a very small cross capacitance betweeen gate $G1$ and dot $D2$ and vice-versa. As the voltage on V_{g1} and V_{g2} increases, the interdot capacitance also increases. This splits the conductance maxima forming a hexagonal domain in the $V_{g1} - V_{g2}$ space. The interdot capacitance C_m has an intermediate value between $0 < C_m < C_{tot1}(C_{tot2})$. This situation is shown in fig. 4.17b. The hexagonal cell is related to the capacitance, and the interdot capacitance

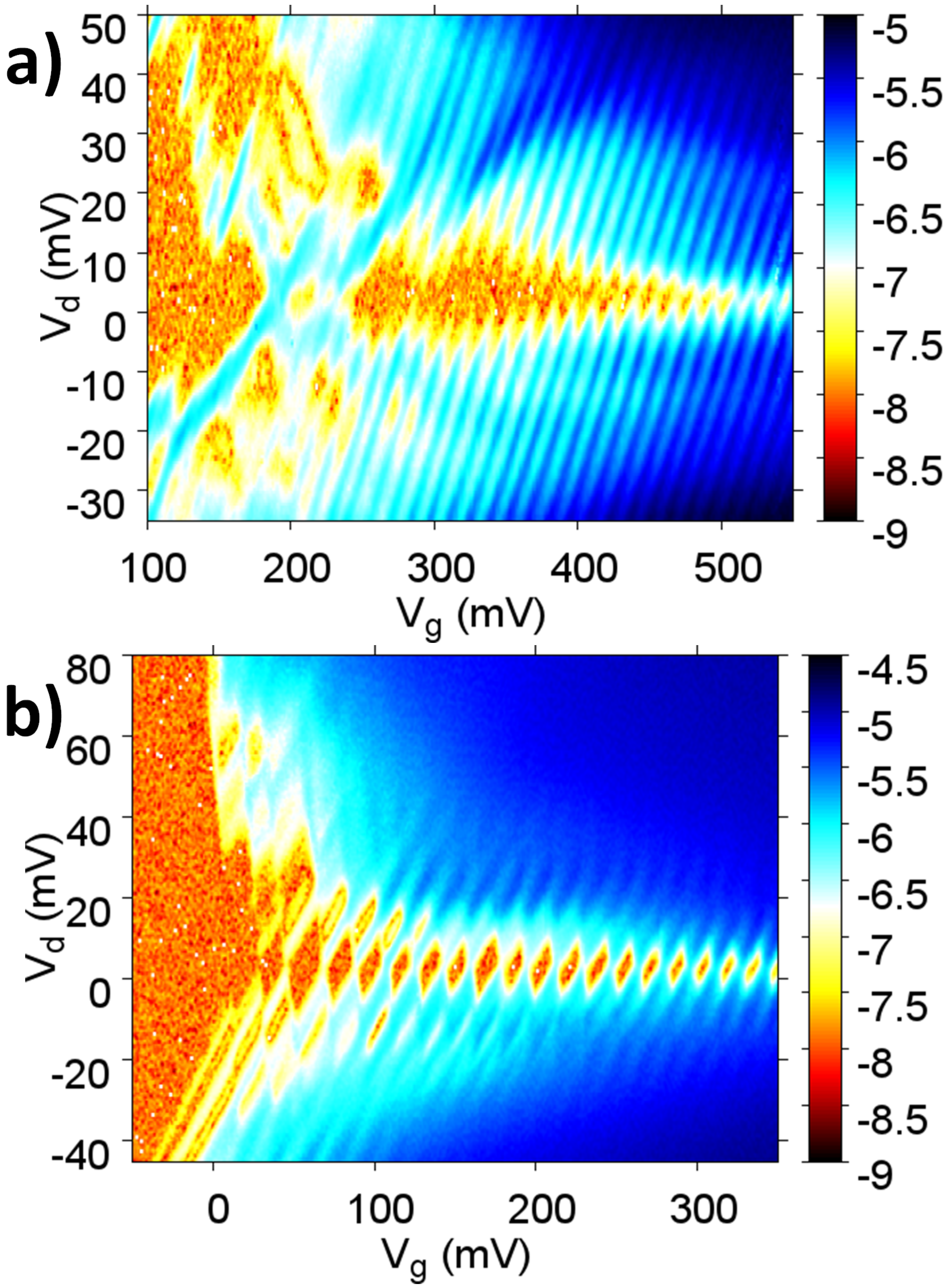

Figure 4.16: a) Differential conductance measurement in the non-linear regime at $4.2K$ for $G1$ holding $G2$ at $1V$. b) Differential conductance measurement in the non-linear regime at $4.2K$ for $G2$ holding $G1$ at $1V$.

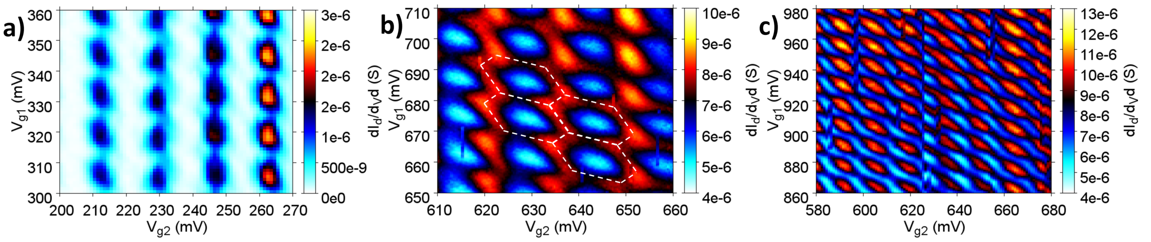

Figure 4.17: Differential conductance at $4.2K$ as a fucntion of V_{g1} and V_{g2}. a) Square conductance pattern in the weak interdot coupling regime, $C_m \sim 0$. b) The square pattern in a) evolves into a honeycomb pattern due to finite interdot capacitance. c) In the limit, $C_m \rightarrow C_{tot1(2)}$ the double dot system behaves as a single big dot with charge $(n_1 + n_2)$ on it.

can be calculated from the dimensions of the honeycomb cell. The charge on each dot within each honeycomb cell is constant and changes only at the triple points. From the dimensions of the honeycomb in fig. 4.11b, $\Delta V_{g1}^{m} = \Delta V_{g1} \frac{C_m}{C_2}$ and $\Delta V_{g2}^{m} = \Delta V_{g2} \frac{C_m}{C_1}$, can be measured which gives the separation between the triple point along V_{g1} and V_{g2} respectively.

As mentioned earlier and depicted in fig. 4.11b, from the geometry of the hexagonal cell the quantity ΔV_{g}^{m} can be determined to

$$\Delta V_{g1}^{m} = 5.7mV$$

and

$$\Delta V_{g2}^{m} = 6.5mV$$

From these the interdot capacitance C_m can be calculated according to eqs. 4.18 and 4.20, yielding $C_m = 7.06aF$ from ΔV_{g1}^{m} and $C_m = 6.73aF$ from ΔV_{g2}^{m} . The difference between C_m calculated for ΔV_{g1}^{m} and ΔV_{g2}^{m} is $0.33aF$ which amounts to approximately 5% of the interdot capacitance calculated. The total capacitance of dot D1 is $24aF$ and that of dot D2 is $22.7aF$. From the interdot capacitance calculated, it can be seen that C_m has a value between 0 and $C_{tot1(2)}$ as expected from the theory. With a further increase in the gate voltage the tunnel barriers are lowered further so that the interdot capacitance C_m becomes the dominant capacitance and the double dot behaves like a single big dot with charge $(n_1 + n_2)$ on it and it is tuned by two gates. This results in a vanishing of the honeycomb pattern and the conductance pattern evolves into diagonal lines with a negative slope. The slope of these lines is given by $\frac{dVg1}{dVg2} = -1$ in case of symmetric capacitive coupling from both gates to the single big dot. Fig. 4.17c shows that the honeycomb structure in fig. 4.17b evolved into diagonal lines with negative slope for higher $G1$ voltages. For increasing $G1$ voltages the barrier betwen dot $D1$ and $D2$ is lowered and at sufficiently high gate voltage the barrier vanishes forming a single big dot as expected from the theory.

We used the capacitance values extracted from the measured honeycomb pattern and performed simulations at $4.2K$. The parameters used for simulation are summarized

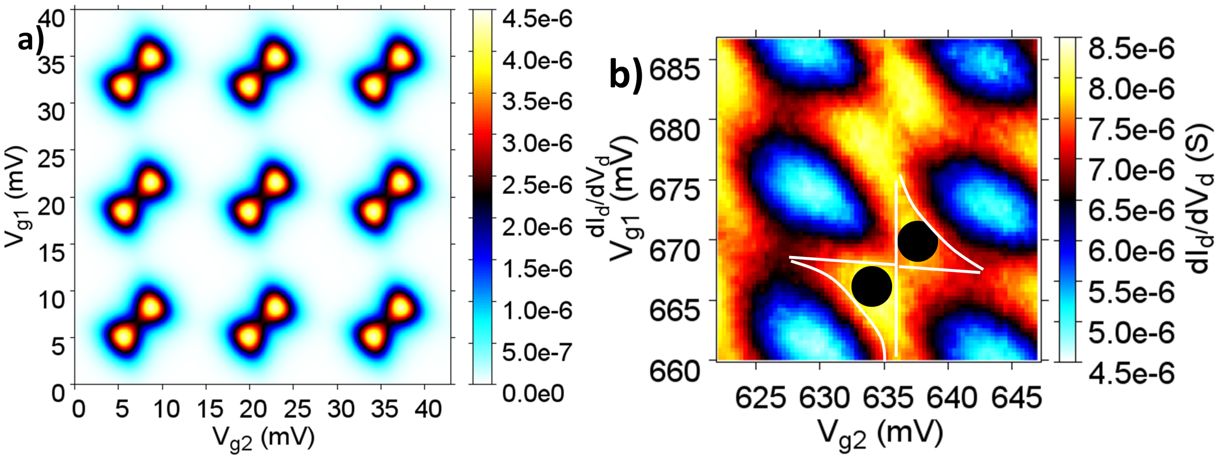

Figure 4.18: a) Simulated charge stability for the parameters extracted from the measured conductance in linear response. b) Finite conductance in the vicinity of triple points due to wavefunction overlap between the two dots. The triple points are marked by black solid circles. The white outlined region in fig. 4.18b shows an extended conductance region.

Capacitor	Capacitance (aF)	Barrier conductance $(\frac{e^2}{h})$ for $V_d = 10^{-4}V$
C_1	5	0.1
C_2	4.5	0.1
C_m	7	0.1
C_{g1}	12	0
C_{g2}	11.2	0
C_{g12}	0	0
C_{g21}	0	0

Table 4.2: Parameters used for simulation in fig. 4.18a.

in table 4.2.The parameters extracted from the measurements generate a honeycomb pattern which agrees well with the dimension of the measured honeycomb pattern. In a double dot system in series, the electrons flow through the device only at the triple points; in other regions the charge is stable on the dots and so no current flows through the system. This can been seen in the simulation shown in fig. 4.18a. But in the measured honeycomb pattern (fig. 4.18b) the current flows even in the region outside the triple points which is absent in the simulation. This is because the simulation is based on a purely electrostatic model and does not take into account quantum mechanical tunneling effects. We can see the current flowing in the region outside the triple points due to the wave function on either dot extended over the other dot leading to a tunnel currrent flow outside the region of triple points [48][49].

4.5 Electron Transport through Triple Dots in Series

4.5.1 Introduction

Electron transport through single [50][51][4] and coupled quantum dots [44][52][53][54] has been studied extensively. Extending the double dot system towards triple dots is

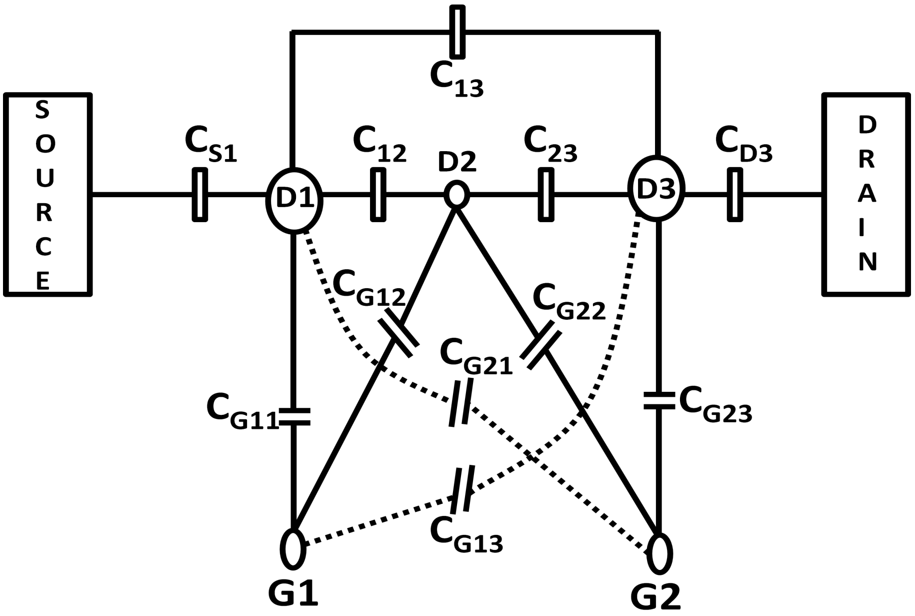

Figure 4.19: Electrostatic circuit diagram for triple quantum dots in series.

a natural step towards multi-dot systems which may find an application in electron pumps, parametron devices [55], rectifier devices [56] and quantum cellular automata [57]. Triple dot configurations have been realized in a two-dimensional electron gas [58][59][60] and in silicon [61][62]. In most of the cases triple dots in series have been studied in a symmetric configuration. In this section, we discuss the effects on transport through asymmetrically coupled triple dots in series. Asymmetry arises from the variation in the gate lengths which effectively changes the capacitive coupling to the dots and results in novel transport properties of the coupled dots. We give an electrostatic model which accounts for the asymmetry and yields a result that agrees well with the experimental data.

4.5.2 Electrostatic Model for Triple Quantum dots in Series

In this section the electrostatic model for triple quantum dots (TQD) in series is considered. The electrostatic model describing the transport of electrons through TQD considered here is purely classical and no quantum mechanical tunneling is explicitly taken into account. Fig. 4.19 shows the electrostatic circuit diagram for the TQD in series. The circuit describes three quantum dots ($D1$, $D2$ and $D3$) tunnel-coupled to each other and the coupling between gates and dots is described by capacitors. Dot $D1$ is tunnel coupled to source and dot $D3$ is tunnel coupled to drain. The tunnel barriers are modelled as an ohmic resistor in parallel with a capacitor. The circuit consists of charge nodes (QDs $D1$,$D2$, and $D3$) and voltage nodes (gates G_1 and G_2) and the capacitors separating the nodes. In this work only the transport in the linear regime is considered i.e. $V_{ds} \approx 0V$.

Using the relation

$$\overrightarrow{Q} = \overrightarrow{C}\,\overrightarrow{V}$$

we can write the charge on charge node and voltage node as follows:

$$\begin{bmatrix} \overrightarrow{Q_D} \\ \overrightarrow{Q_V} \end{bmatrix} = \begin{bmatrix} C_{DD} & C_{VD} \\ C_{VD}^T & C_{VV} \end{bmatrix} \begin{bmatrix} \overrightarrow{V_D} \\ \overrightarrow{V_V} \end{bmatrix} \tag{4.36}$$

where the subscript D denotes the charge node, the subscript V denotes the voltage node and

$$\overrightarrow{Q_D} = \begin{bmatrix} Q_1, & Q_2, & Q_3 \end{bmatrix}^T$$

is the total charge on the charge node (quantum dots) $D1$, $D2$ and $D3$ respectively,

$$\overrightarrow{Q_V} = \begin{bmatrix} Q_{G1}, & Q_{G2} \end{bmatrix}^T$$

is the charge on the voltage nodes (gates) $G1$ and $G2$ respectively,

$$\overrightarrow{V_D} = \begin{bmatrix} V_{D1}, & V_{D2}, & V_{D3} \end{bmatrix}^T$$

is the voltage on the charge nodes $D1$, $D2$ and $D3$ respectively and

$$\overrightarrow{V_V} = \begin{bmatrix} V_{G1}, & V_{G2} \end{bmatrix}$$

is the voltage on the voltage nodes $G1$ and $G2$ respectively. The superscript T represents the transpose of the matrix.

The total capacitance on the systtem is divided into two parts: One containing only the capacitances between the quantum dots given by

$$C_{DD} = \begin{bmatrix} C_{\Sigma 1} & -C_{12} & -C_{13} \\ -C_{12} & C_{\Sigma 2} & -C_{23} \\ -C_{13} & -C_{23} & C_{\Sigma 3} \end{bmatrix}$$

where $C_{\Sigma i}$ is the total capacitance on the dot i, where $i = 1, 2$ or 3, and C_{ij} is the interdot capacitance between the dots i and j, where i and $j = 1\,2\,\mathrm{or}\,3$ and $i \neq j$, and second containing those between the gates $(G1\,\mathrm{or}\,G2)$ and quantum dots $(D1, D2\,or\,D3)$:

$$C_{VD} = \begin{bmatrix} -C_{G11} & -C_{G21} \\ -C_{G12} & -C_{G22} \\ -C_{G13} & -C_{G23} \end{bmatrix}$$

For simplicity, we set the capacitances between the voltage sources to zero, i.e. $C_{VV} = 0$ without the loss of generality.

The free energy of the system is given by [59]:

$$F = U - W \tag{4.37}$$

where U is the electrostatic energy and W is the work done.

$$F = \frac{1}{2}\left[Q_D^T, Q_V^T\right]\begin{bmatrix} V_D \\ V_V \end{bmatrix} - V_V^T Q_V$$

According to [59], the above equation can be transformed into:

$$F = \frac{1}{2}\left(C_{DD}^{-1} Q_D^{eff}\right)^T Q_D^{eff}$$

$$F = \frac{1}{2e^2} Q_1^{eff}\left(E_1 Q_1^{eff} + E_{12} Q_2^{eff} + E_{13} Q_3^{eff}\right)$$

$$+ \frac{1}{2e^2} Q_2^{eff}\left(E_{12} Q_1^{eff} + E_2 Q_2^{eff} + E_{23} Q_3^{eff}\right)$$

$$+ \frac{1}{2e^2} Q_3^{eff}\left(E_{13} Q_1^{eff} + E_{23} Q_2^{eff} + E_3 Q_3^{eff}\right) \tag{4.38}$$

where $Q_x^{eff} = Q_x + C_{x1}V_1 + C_{x2}V_2 + C_{x3}V_3$ and the charging energies of the individual quantum dot is given by [59]:

$$E_x = K\left(C_{\Sigma y} C_{\Sigma z} - C_{yz}^2\right) \tag{4.39}$$

$$E_{xy} = K\left(C_{\Sigma z} C_{xy} + C_{xz} C_{yz}\right)$$

where

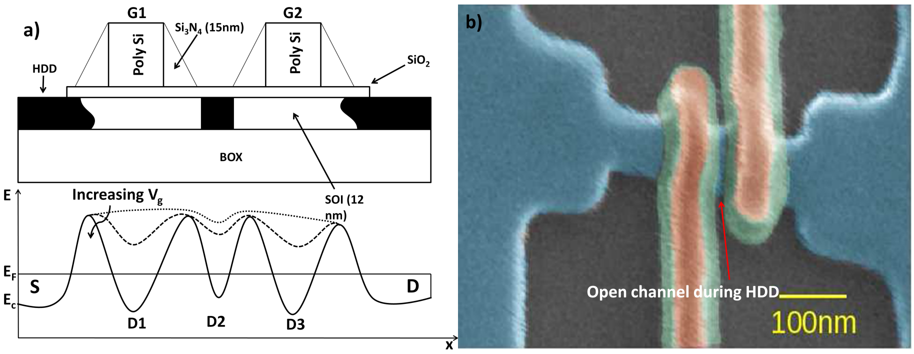

Figure 4.20: a) Top: Schematic of the device. Bottom: the bottom of the conduction band is drawn for various gate voltages. The horizontal line is the Fermi energy fixed by source and drain. b) Colored SEM top view showing a nanowire with two gates and $15nm$ thick spacers. Blue is SOI, red is polysilicon gate and green are nitride spacers.

$$K = \frac{e^2}{C_{\Sigma 1}C_{\Sigma 2}C_{\Sigma 3} - 2C_{12}C_{13}C_{23} - C_{\Sigma 3}C_{12}^2 - C_{\Sigma 2}C_{13}^2 - C_{\Sigma 1}C_{23}^2} \tag{4.40}$$

and x, y, z stands for cyclic permutation of dot $D1$, $D2$ and $D3$ and $C_{\Sigma 1}$, $C_{\Sigma 2}$ and $C_{\Sigma 3}$ are the total capacitances of the dots while C_{12} , C_{23} and C_{13} are the interdot capacitances. Eq. 4.38 will be used to calculate the charging energy of individual dot in our system.

4.5.3 Fabrication of the Device

Fig. 4.20a shows the schematic of the device. To fabricate the device with three dots in series first silicon is thinned down to $12nm$ silicon. Then two polysilicon gates of $50nm$ length are deposited on the wire above an SiO_2 gate oxide layer of $5nm$ (fig. 4.20a). The lateral separation between the two gates is $50nm$. Silicon nitride spacers of $15nm$ width are deposited on both sides of the gates leaving a $20nm$ gap. Heavy As implantation is performed (HDD) to form a self-aligned source and drain reservoir using the gates and spacers as masks. In our device, the region below the gates, $G1$ and $G2$ form quantum dots, $D1$ and $D3$, respectively, upon application of positive voltages on the gates, whereas the regions below the spacers form barriers between the dots. The $20nm$ long channel section between the gates is also heavily doped which leads to formation of a third dot $(D2)$ in the region between the two gates. The shape of the bottom of conduction band which forms the central dot $D2$ depends on the distribution of the dopants from HDD in the central region of the channel. We assume that the doping is maximum in the central region and decraeses gradually on both the sides which gives us the potential as shown in fig. 4.20a (bottom). Fig. 4.20b shows the SEM images of a similar device showing an open channel section between the two gates which is doped during the HDD.

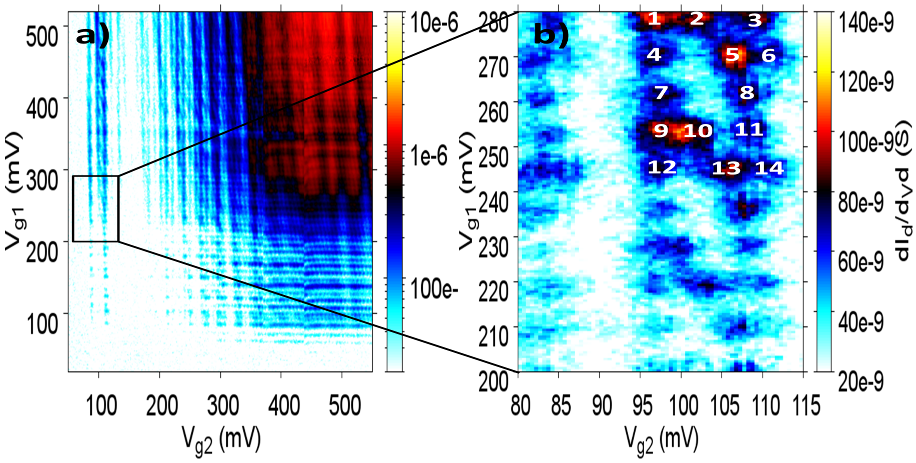

Figure 4.21: a) Differential conductance measurement at $4.2K$ in the $V_{g1} - V_{g2}$ space in the linear regime. b) Small region from a) with high resolution measurement.

4.5.4 Measurements

All measurements in this work were performed at the ^4He bath temperature, $(T = 4.2K)$. To measure the conductance of the device, a small ac excitation voltage, typically $50\mu V$, was applied between the source and drain reservoirs and low-frequency $(f = 27.3Hz)$ phase-sensitive detection was used. Fig. 4.21a shows the 2-D plot of the conductance in $V_{g1} - V_{g2}$ plane. Coulomb oscillations along V_{g1} and V_{g2} are visible due to the weak interdot capacitance between $D1$ and $D3$ as indicated by points 3, 4, 7, 8, 11 and 12 in fig. 4.21b. At these points, electrons tunnel from dot $D1$ to dot $D3$ directly without adding electron to dot $D2$. The period of oscillations for $D1$ is $\sim 7.6mV$ and for $D2 \sim 11.4mV$, which corresponds to gate capacitances of $21aF$ and $14aF$, respectively. In fig. 4.21b we can notice that due to a large distance between $D1$ and $D3$ compared to the distance between $D1$ and $D2$ or $D2$ and $D3$ the conductance at points 3, 4, 7, 8, 11 and 12 is less than at points 1-2, 5-6, 9-10 and 13-14. The reason for reduced conductance at points 3, 4, 7, 8, 11 and 12 is that the tunneling current decreases exponentially with increasing distance between two dots. In addition to Coulomb oscillations due to electron tunneling from $D1$ to $D3$ we also see an additional feature every third oscillation along V_{g1} and every second oscillation along V_{g2} which is thought to be due to an electron added to the $D2$ (points 1-2, 5-6, 9-10 and 13-14 in fig. 4.21b). This indicates that the ratio of capacitive coupling between $G1$ and $D1$ and $G1$ and $D2$ is 3. Similarly, the ratio of the capacitive coupling between $G2$ and $D3$ and $G2$ and $D2$ is 2. Therefore, capacitance between $G1$ to $D2$ is $7aF$ and between $G2$ to $D2$ it is also $7aF$. The fact that C_{g23} is only $\frac{2}{3}$ of C_{g11} may be caused by a shorter gate length for $G2$. Such a variation in the gate length is evident from the room temperature conductance measurement (fig. 4.22) as a function of gate voltage for a small ac voltage applied to source-drain. The subthreshold slope of $G2$ is $\sim 226mV/decade$ whereas for $G1$ it is $\sim 151mV/decade$. This smaller effect of $G2$ may be caused by a shorter gate length.

Based on the conclusions drawn from the measured charge stability diagram, simulations have been performed. Table 4.3 shows the capacitance and barrier conductance values used for the simulation. Fig. 4.23 shows the schematic diagram which explains

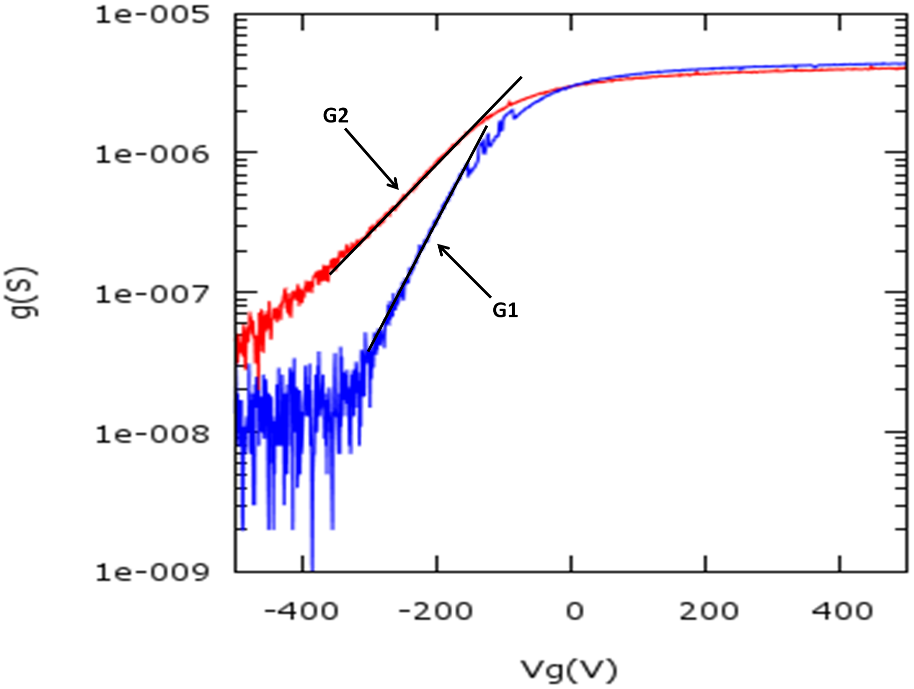

Figure 4.22: Room temperature characterization of each gate. Black lines indicate different subthreshold slopes for each gate. *G*2 has a larger subthreshold slope due to smaller gate length.

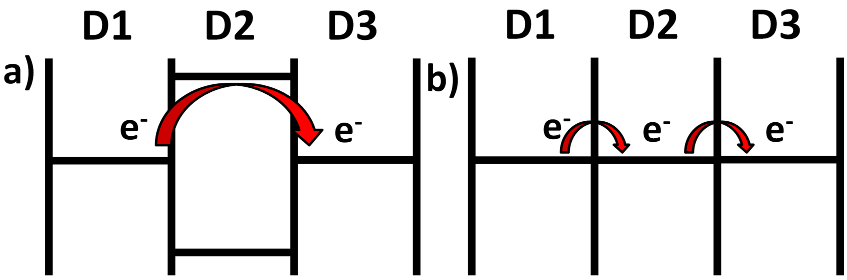

Figure 4.23: a) Schematic explanation of electron transport when *D*2 is not in resonance with *D*1and *D*3. b) Schematic explanation of electron transport when *D*1, *D*2 and *D*3 are in resonance.

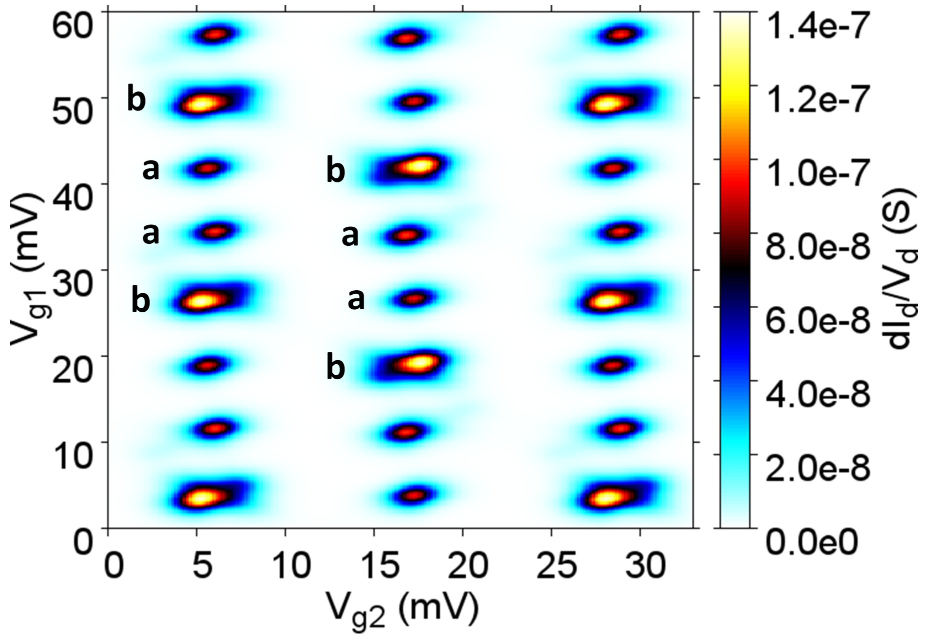

Figure 4.24: Simulated charge stability diagram at 4.2K for the parameters extracted from the measured charge stability diagram.

Capacitor	Capacitance (aF)	Barrier Conductance ($\frac{e^2}{h}$) for $V_d = 10^{-4}V$
C_{S1}	2	0.4
C_{D3}	2	0.4
C_{12}	2	0.4
C_{23}	2	0.4
C_{13}	0.05	0.05
C_{G11}	21	0
C_{G12}	7	0
C_{G22}	7	0
C_{G23}	14	0
C_{G13}	0	0
C_{G21}	0	0

Table 4.3: Capacitance values used for simulation in the fig. 4.25.

the electron tunneling across the device. As the gate voltages V_{g1} and V_{g2} are swept in the positive direction, this lowers the energy levels in the dots. With positive application of V_{g1} this aligns the energy level of $D1$ with the source. Hence, an electron tunnels from the source onto $D1$. If at this time there is an energy level on $D3$ aligning with $D1$ but no energy level on $D2$ aligning with $D1$, the electron tunnels from $D1$ to $D3$ as shown in fig. 4.23a. This tunneling process from dot $D1$ to dot $D3$ leads to conductance oscillations at points a in fig. 4.24. But when the energy level of $D2$ is aligned with the energy level of $D1$, then the electron tunneling from $D1$ to $D3$ takes place via $D2$, as shown in fig. 4.23b. This tunneling process leads to conductance oscillations at points b in fig. 4.24. As can be seen from fig. 4.24, the charge stability diagram resulting from the simulation using the parameters from table 4.2 agree very well with the experimental charge stability in fig. 4.21b. The total capacitance and the charging energy of each dot are summarized in table 4.3.

Dot number	Total Capacitance (aF)	Charging energy (meV)
D_1	25.05	5.6
D_2	18.00	8.0
D_3	18.05	7.9

Table 4.4: Total capacitance and the charging energy of individual dot calculated using eq. 4.38.

To conclude, we have studied an asymmetrically coupled triple dot in series configuration where three dots are controlled by two gates. It consists of two dots in series separated by a piece of locally doped silicon nanowire forming a third dot.

4.6 Multi-gate Devices

Section 4.2 discusses the formation of the quantum dots for the devices studied in this work. From fig. 4.2a we can see that the doping level along the length of the channel is not uniform. The region of source and drain is highly doped, forming metallic contacts, whereas the region below the spacers is lowly doped. The region below the gate is undoped which forms the quantum dot upon application of a positive voltage. Due to this doping gradient, the dopants from the source and drain diffuse towards the center of the channel. This makes the region below the spacer lowly doped. Hence, upon application of a positive voltage on the gate, the region below the spacers forms barriers separating the dot from the source and drain. In the large spacer $(40nm)$ devices, the possibility of the region below the gate remaining undoped is high but in small spacer $(15nm)$ devices, chances that the dopants diffuse into the central region of the channel are high. In such a case, the transport through the device depends strongly on the nature of the dot formed. Diffussion of dopants in the channel may lead to a potential fluctuation resulting in the formation of a disordered dot. In the single top gate devices investigated so far, the transport properties exhibited were compatibe with the formation of a single dot below the gate. In this section, we discuss the effect of the dopant diffusion into the channel forming a disordered dot behaving as a coupled dot system [63][64].

Fig. 4.25 shows the device geometry. In addition to a top gate, the device also has two side gates which can be used to study the coupling between the dot and the dopants in the vicinity. Fig. 4.26a shows the differential conductance measurement at $4.2K$ as a function of V_{tg} and V_{sg2} in the linear regime, where V_{tg} is the voltage applied on the top gate and $V_{sg1(2)}$ is the voltage applied on side gate $sg1(2)$. The inset in fig. 4.27a shows a single trace of dI_d/dV_d as a function of V_{tg}. For $V_{sg2} = 0mV$, the trace shows clear Coulomb oscillations. The line widths of the Coulomb oscillations are not identical. In addition, beyond $V_{tg} = 200mV$ we see peak splitting. Also, for a single quantum dot, conductance measurement in $V_{tg} - V_{sg2}$ plane would show conductance lines with negative slope (see section 4.3, e.g. fig. 4.10c). The conductance measurement as a function of $V_{tg} - V_{sg2}$ in fig. 4.26a does not show lines, instead we can see an additional feature. Fig. 4.26b shows a magnified region of fig. 4.26a. We clearly see a large number of honeycomb patterns which is essentially a feature of a double dot system. The conductance at the triple points is thermally broadened. Fig. 27a

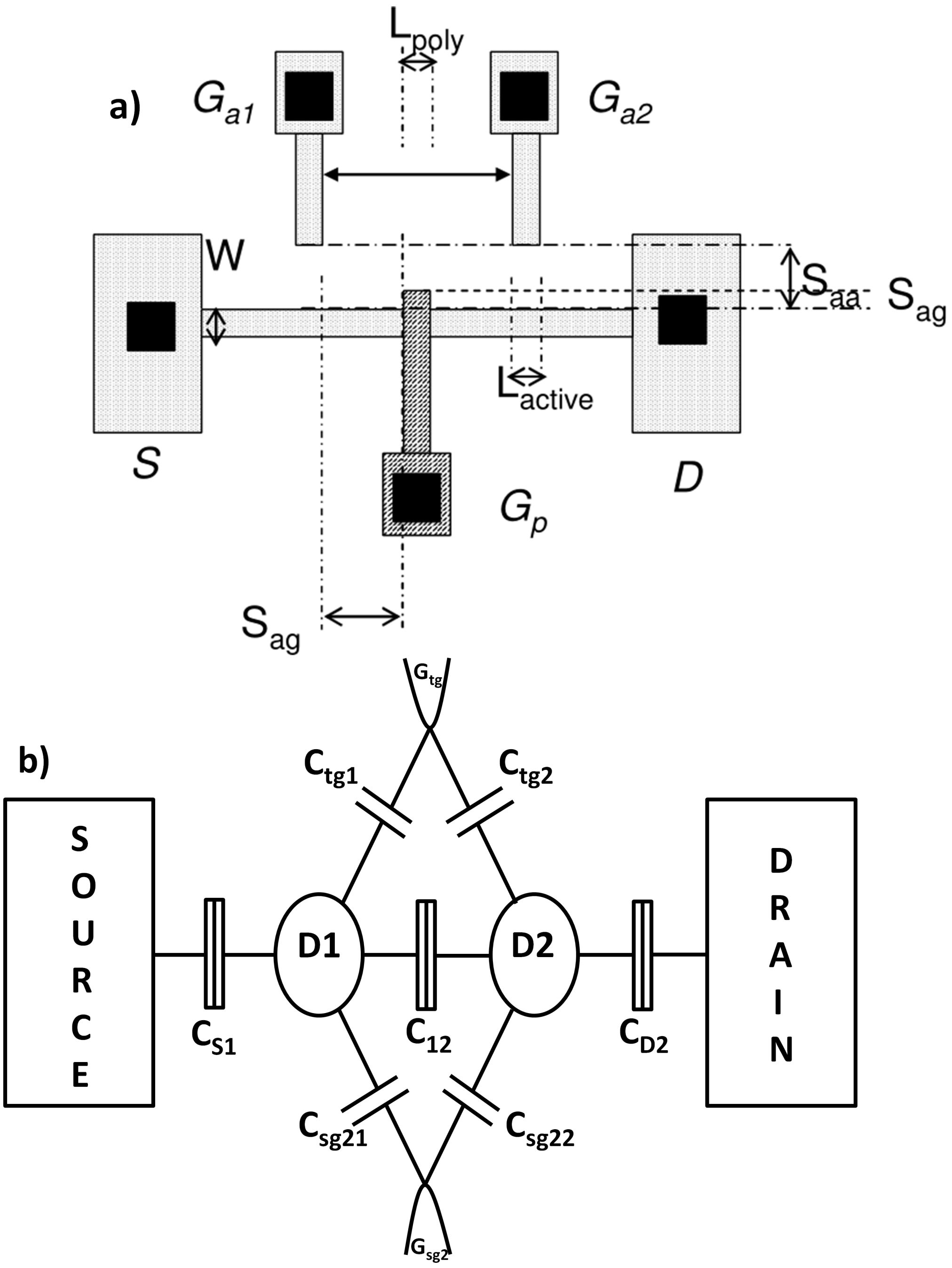

Figure 4.25: a) Geometry of the device used to study the interaction of the dot formed below the gate (intentionally formed quantum dot) with its background. b) Electrostatic model considered for the simulations performed.

Capacitor	Capacitance (aF)
C_{S1}	5
C_{D2}	5
C_{tg1}	10.6
C_{tg2}	8
C_{sg12}	0.215
C_{sg22}	0.43
C_{sg21}	0.02
C_{sg12}	0.02
C_{12}	1.5

Table 4.5: Capacitance values extracted from the measured data.

shows the conductance measurement in the linear regime as a function of V_{tg} and V_{sg2} at $T = 1.5K$. Clearly, the thermally broadened triple points in fig. 4.26a are now clearly visible and the conductance outside the vicinity of triple points is completely suppressed. Fig. 4.27b shows conductance measurement as a function of $V_{tg} - V_{sg1}$ at $T = 1.5K$. Comparing the dimensions of the honeycombs in fig. 4.27a and in fig. 4.27b, we see that the size of the honeycomb in fig. 4.27a in V_{sg2}-direction is half that in fig. 4.27b. From the honeycomb pattern, all the capacitance can be extracted (see fig. 4.27a). The capacitance values for both the measurements are summarized in table 4.4 . These coupled dot features seen in the measurement indicate that the dopants from the source and drain have diffused into the channel, which results in a multi-dot structure (electrostatic model considered for this device is shown in fig. 4.25b). From the capacitance values in the table 4.4, we can see that the top gate coupled much more strongly to both the dots compared to the side gates. Also the capacitive coupling between the top gate and both the dots is of similar strength. This suggests that both the dots are formed below the top gate which results in a strong capacitive coupling with the top gate.

To conclude, we have studied electron transport through multi-gate device, with single top gate and two side gates. We measured conductance through the device in the linear regime as a function V_{tg} and V_{sg} at $4.2K$ and at $1.5K$ and show that due to diffusion of dopants in the central region of the channel, a disordered wire is formed leading to electron transport through multi-dot structure.

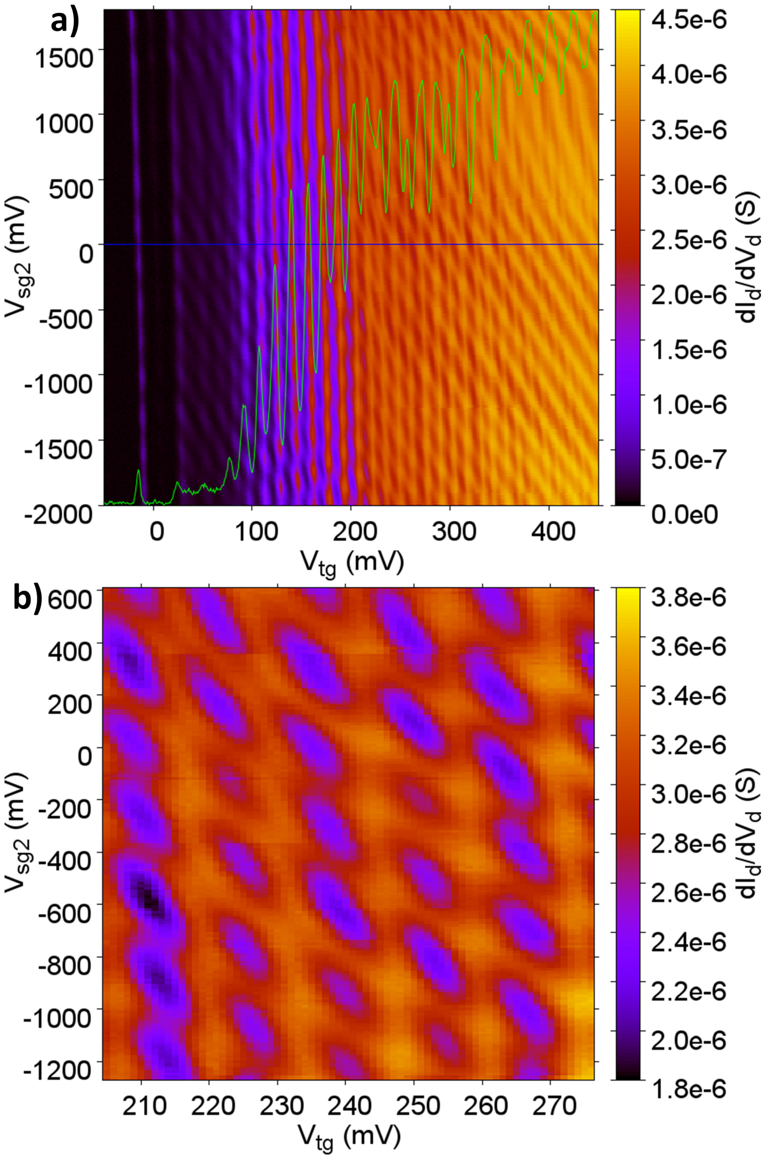

Figure 4.26: a) Conductance measurement at $4.2K$ in the $V_{tg} - V_{sg2}$ space. Inset shows a trace at $V_{sg2} = 0V$. Blue line represents the position at which the trace is taken. b) Magnified region from a) clearly showing honeycomb patterns.

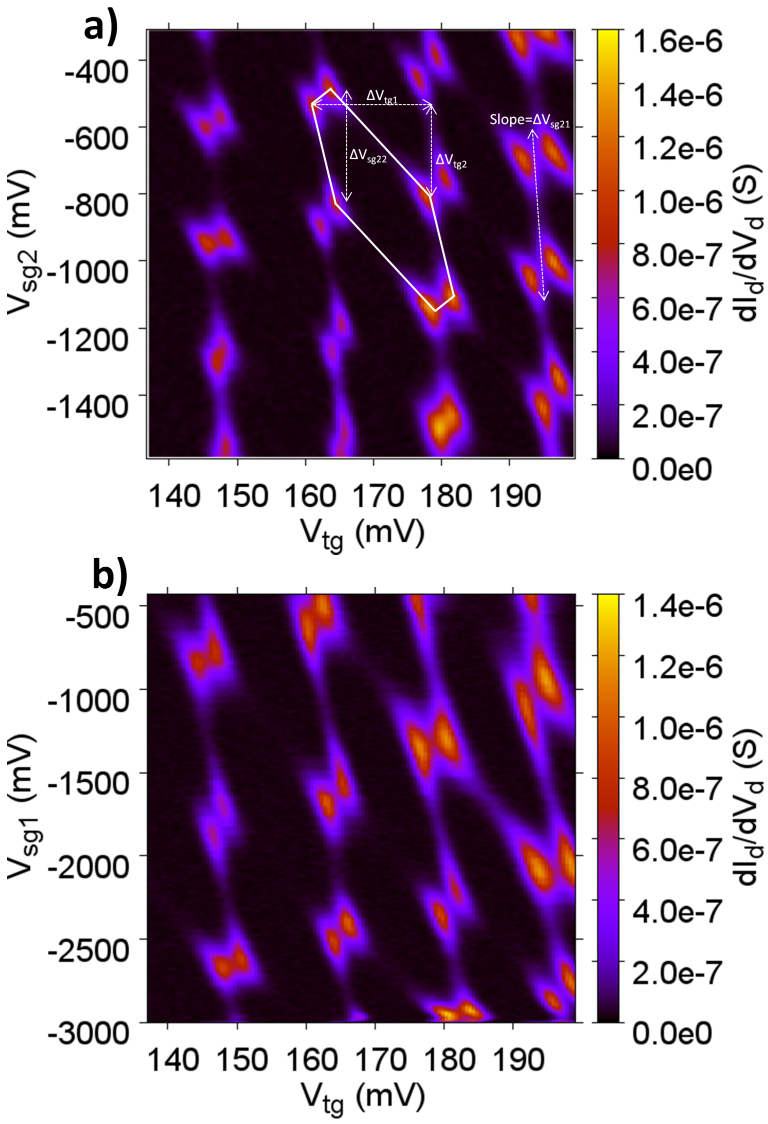

Figure 4.27: a) Conductance measurement as a function of $V_{tg} - V_{sg2}$ at $1.5K$. b) Conductance measurement as a function of $V_{tg} - V_{sg1}$ at $1.5K$.

Chapter 5

Charge Granularity in Single Electron Transistors

5.1 Introduction

SETs have been demonstrated using different techniques to define a nanoscale islands with tunnel barriers, e.g. doped single crystal silicon wires with constrictions [65][66], polysilicon nanowires [67][68][69], and MOSFET structures [70][71][72]. In polysilicon wire devices, individual grains act as islands and grain boundaries as tunnel barriers, whereas in MOSFET structures islands and barriers are formed by doping modulation along the length of the wire. SETs are extremely sensitive to small changes in charge in their environment [73]. In this chapter we discuss the charging effects in polysilicon gates. These charging effects become visible at low temperature. They are sensed by the quantum dot formed in the silcion channel below the gate giving rise to novel features.

5.2 Measurements

All the measurements presented in this chapter were performed at $4.2K$ in a helium dewar and in a dilution refrigerator at a bath temperature of $1K$ and $70mK$. Two methods were used for the measurements. In one, a small ac excitation voltage, typically $50\mu V$, was applied between source and drain reservoirs and the conductance through the device was measured using low frequency $(27.3Hz)$ phase-sensitive current detection (differential conductance). In the second method a small ac excitation was applied to the gate electrode and conductance through the device was measured using the same low frequency phase-sensitive detection (transconductance). Two types of devices are studied: A) a device with a single top gate and B) a device with a single top gate and two side gates. Type B devices give additional freedom to study the electron transport in linear response as a function of side gates. Fig. 5.1 shows the geometry of type B devices. Type A samples have similar geometry but do not have the gates G_{a1} and G_{a2}. The side gates are $50\,nm$ away from the wire. Type A samples will be used to study the conductance in a non-linear regime using a differential conductance and a transconductance measurement set-up whereas with type B samples in additon, conductance can be studied in a linear regime as a function of side gates.

Fig. 5.2 shows the result of differential conductance and of transconductance measurements in a type A sample with a gate length of $L_g = 30nm$, a wire width of $W =$

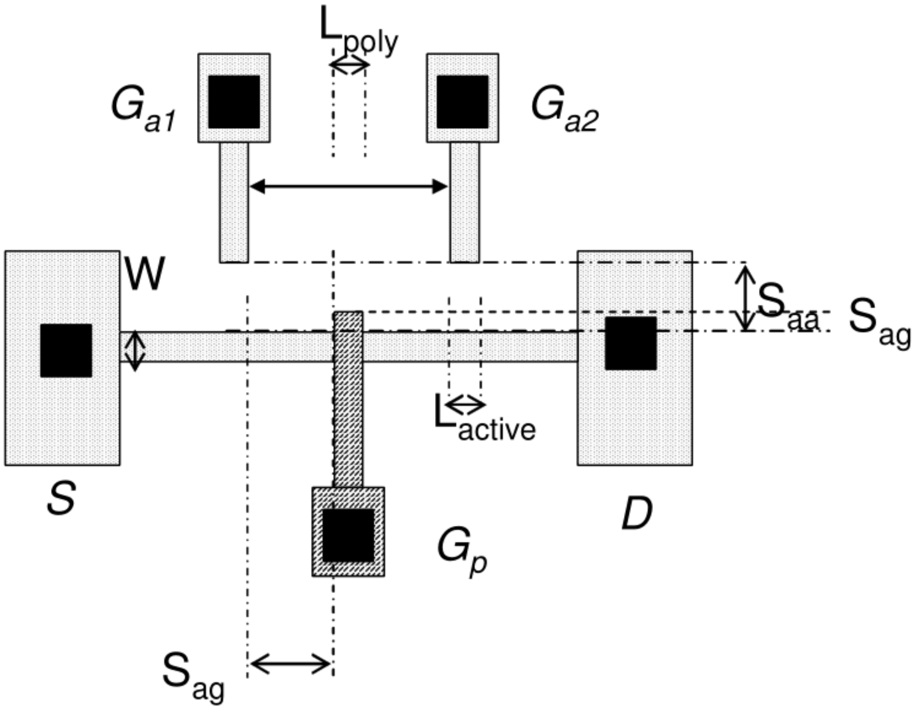

Figure 5.1: Device geometry of type B (same as fig. 4.25a).

$60nm$, a wire thickness of $t_{Si} = 8nm$ and a spacer width of $t_{spacer} = 25nm$. Clear Coulomb blockade diamonds are visible due to the dot formed below the gate ($D1$ in fig. 5.4). In addition to Coulomb diamonds, a large number of conductance lines with a positive slope are also clearly visible. Typical spacings between these lines are $1-2mV$ and the slope of these lines is greater than 1. In the differential conductance measurement (fig. 5.2a), positive differential conductance lines are visible on the positive slope edges of the Coulomb diamonds and negative differential conductance lines on the negative slope edges of the Coulomb diamonds. On the other hand, in the transconductance measurement (fig. 5.2b), negative transconductance lines are visible on the positive slope edges of the Coulomb diamonds and positive transconductance lines on the negative slope edges of the Coulomb diamonds. The usual explanation for conductance lines running along the edges of a Coulomb diamond are excites states (ES) or density of states (DOS) in the electrodes namely, the source or the drain [74]. Other origins could be due to phonon emission and absorption or vibrational states in quantum dots [75]. The ES model is based on the existance of well resolved excited energy levels in the quantum dot due to the confinement of electrons in a small volume. The ES are visible in the conductance measurement if the thermal energy is lower than the mean spacing between the energy levels. An ES model predicts only positive differential conductance because the ESs lie at an energy higher than the ground state. Hence, we expect that the higher energy levels should be more tunnel-coupled to the electrodes since the gate has control over the barriers in the devices studied in this work. Even for equal tunnel-coupling of the ground and the ES to the source and drain electrode the differential conductance is always postive. In order to see negative differential conductance in an ES model the ESs must be less conducting than the ground state [76][77]. Also from our previous discussion of the excited states in quantum dots (see chapter 4, section 4.2), the ES conducntance lines are running parallel to the edges of the Coulomb diamond and the positive slope of the ES conductance lines are less than

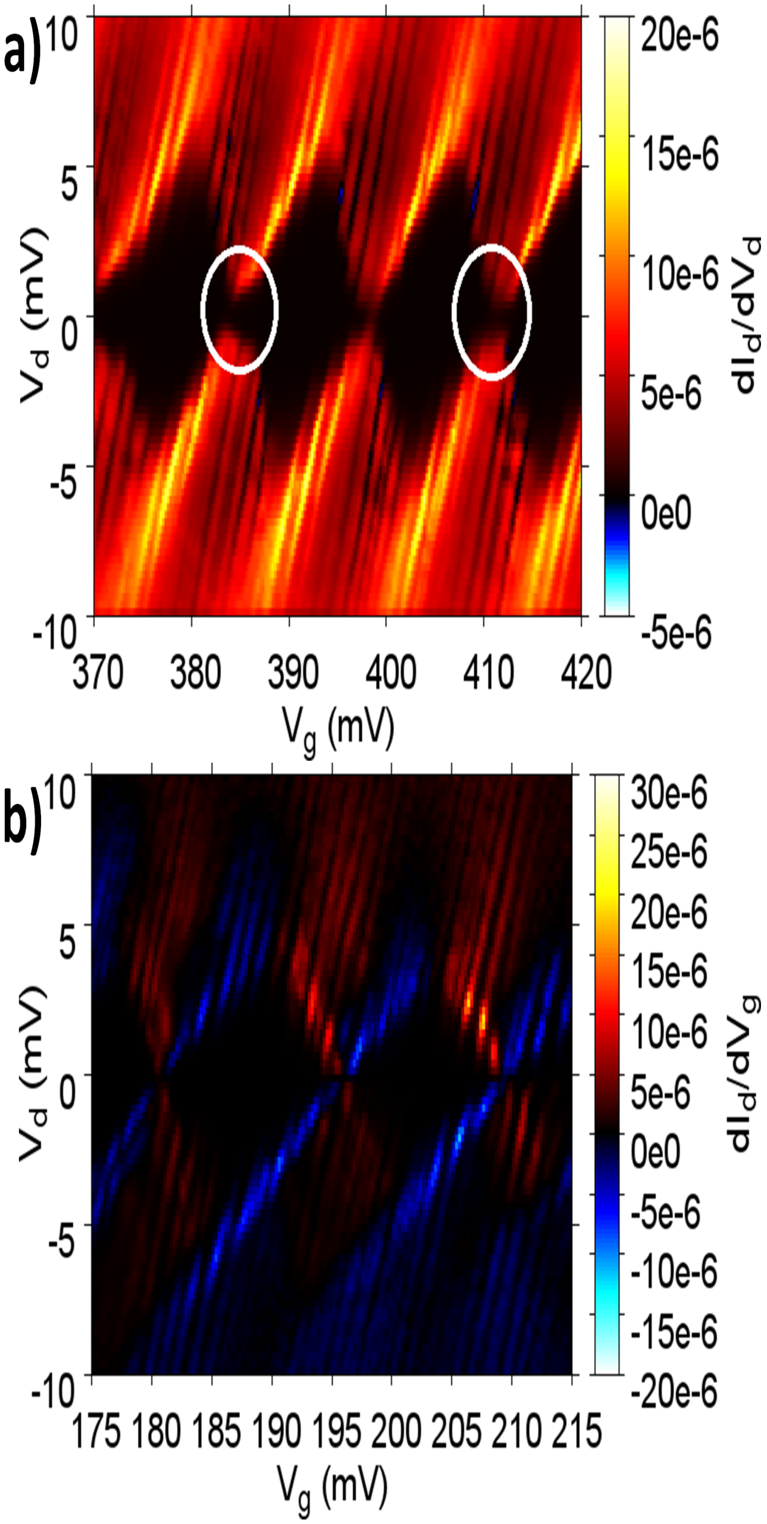

Figure 5.2: a) Differential conductance measurement at $T = 70mK$ for a device with dimensions $L = 30nm$, $W = 60nm$, $Tsi = 8nm$ and $t_{spacers} = 25nm$. b) Transconductance measurement at $T = 70mK$ for the same device as in a). In addition to Coulomb blockade diamonds, lines with slope > 1 are clearly visible.

unity. Hence, the origin of the conductance lines with slope greater than unity as well as the origin of positive and negative conductance lines cannot be explained by the ES model. In the DOS model the same pattern is seen on successive Coulomb diamonds since the gate voltage does not have control over the energy in the source and drain electrodes [78][79]. In this model the conductance through the device is proportional to the local density of states $\nu_{S,D}$ in the source and drain electrode. If the conductance is dominated by the source-dot tunnel barrier then the conductance is proportional to $\frac{d\nu_S}{dE}$ and differential conductance lines running parallel to positive slope of Coulomb diamonds are expected. Similarly, if the conductance is dominated by the drain-dot tunnel barrier then the conductance is proportional to $\frac{d\nu_D}{dE}$ and differential conductance lines are expected along the negative slope of the Coulomb diamond. The DOS model explains the origin of negative differential conductance as the sign of $\frac{d\nu_{S,D}}{dE}$ changes and predicts an equal number of positive and negative differential conductance lines. Even though the DOS model can explain the origin of positive and negative differential conductance lines, it cannot explain the origin of a conductance lines with positive slope greater than unity. Such slopes are unusual because they contradict the basic model of Coulomb charging of a single electron island. The non-linear conductance for a single island, tunnel-coupled to a source and a drain (where the source is grounded and bias is applied to the drain) and capacitively coupled to a gate electrode is expected to show the generic Coulomb diamonds with positive slope dV_d/dV_g always less than unity. A possible explanation for these additional lines in the conductance data would be the existence of an additional island ($D2$ in fig. 5.4). The period of these additional lines suggests that the size of $D2$ is much bigger than the expected size of $D1$. Furthermore, we expect $D2$ to be capacitively coupled to source and drain, otherwise in the non-linear regime the conductance would increase through these lines which is not observed in our measurements. This suggests that the origin of these lines is extrinsic to the SET. We attribute these lines to the charging of polysilicon grains in the gate ($D2$ in fig. 5.4). At sufficiently low temperatures, if the charging energy of the polysilicon grain is larger than k_BT and the resistance of the grain boundaries, R_g is larger than $\frac{h}{e^2}$, the quantum of resistance, the charging of the polysilicon grains is dominated by the Coulomb blockade [13]. Hence, in order to see charging effects in the polysilicon grain, two conditions must be satisfied:

$$E_c > k_BT \tag{5.1}$$

and

$$R_g > \frac{h}{e^2} \tag{5.2}$$

5.3 Grain Boundaries in Polysilicon

Conduction through polysilicon is strongly affected by the potential barriers formed by grain boundaries. These barriers are formed by trap states caused by defects at the boundaries. These trap states capture free carriers in the grain and reduce the carrier density inside the grain. This results in a space charge region around the grain boundary. This space charge region creates an electric field resulting in a Schottky-like potential barrier at the grain boundary. The height and the width of the potential barrier depend on the doping concentration in the grains [80][81][13].

Fig. 5.3 shows schematically a grain of size D and grain boundaries which are thin compared to the size of the grain. The donar concentration is denoted by N_D and is assumed to be uniform whereas the trap density is denoted by N_t at an energy E_t relative to the Fermi level E_F. Electrons from the ionized donors are trapped in the trap states at the grain boundaries. For a low donor concentration N_D, all the electrons may be trapped in the grain boundaries and the grain is depleted. The electric field is generatred by the electrons at the grain boundaries and the ionized donors which results in a potential barrier of height E_{GB}. With an increase in N_D, more charges are trapped in the grain boundaries resulting in an increase in the electric field. Hence, the potential barrier height increases until at $N_D \approx \frac{N_t}{D}$, all the traps are filled and free carriers can exist in the grain, i.e. the conduction band in the center of the grain lies near the Fermi energy E_F. Application of postive voltage on one side of the grain results in the lowering of the conduction band. This results in the lowering of the barrier as well. At sufficiently high positive voltage, thermal emission over the barrier as well as tunneling through its top becomes possible. Hence, electrons transport sets on.

5.4 Electrostatic Model

We propose an electrostatic model based on the conclusions drawn from the measurements. For simplicity, only a single polysilicon grain is assumed to be capacitively coupled to the dot $D1$. The electrostatic model resembles a SEB capacitively coupled to an SET [15] where $D1$ is tunnel-coupled to source and drain and capacitively coupled to $D2$, whereas $D2$ is capacitively coupled to source, drain and $D1$ and tunnel-coupled to the gate (fig. 5.4). If we assume that $D2$ is much larger than $D1$, the effect of charging $D1$ seen by $D2$ is comparatively small. Therefore, for simplicity the electrostatic problem can be solved for the SEB independent of the SET. The electrochemical potential of $D2$ is given by [11]:

$$\mu_{D2} = \frac{(en_2)^2}{C_{\Sigma 2}} - \frac{e\,(C_{S2}V_s + C_{D2}V_d + C_{G2}V_g)}{C_{\Sigma 2}} \tag{5.3}$$

where $C_{\sum 2} = C_{S2} + C_{D2} + C_{G2}$ assuming C_{dd} is very small compared to C_{S2}, C_{D2} and C_{G2} and n_2 is the electron number on the dot $D2$. Since $D2$ is tunnel-coupled to the gate, the charge on $D2$ changes by 1 when the electrochemical potential of the gate

$$\mu_g = \mu_{g0} - eV_g \tag{5.4}$$

(where μ_{g0} is the electrochemical potential of the gate when no gate voltage is applied)

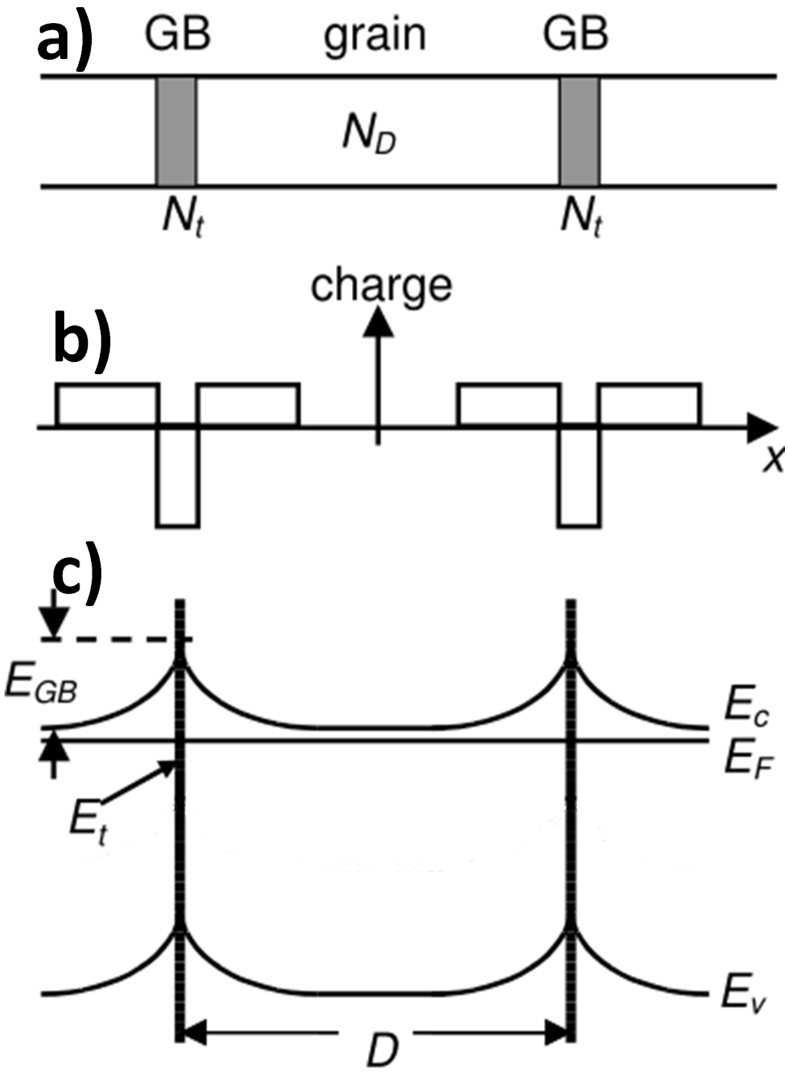

Figure 5.3: a) Schematic diagram of a polysilicon grain isolated by grain boundary. N_t is the trap density per unit area. b) Charge density across the grain and the grain boundary. c) Energy band diagram along the grain and grain boundary. Image taken from ref. [13].

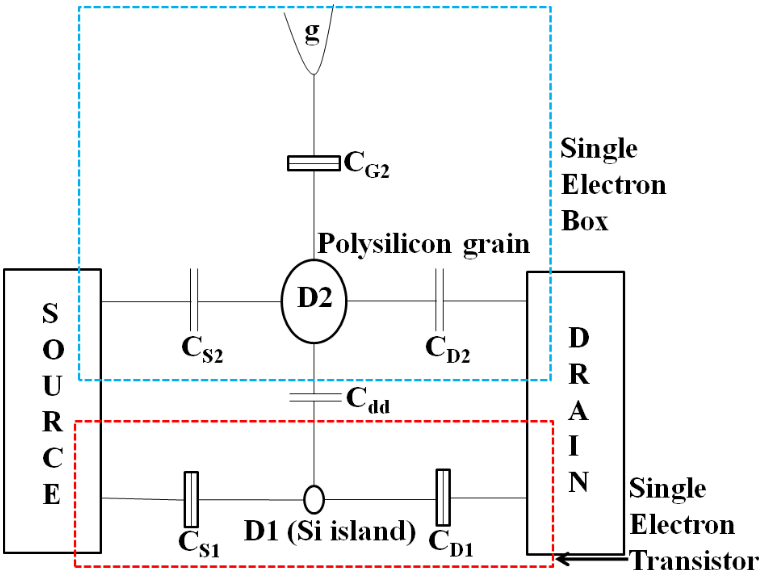

Figure 5.4: Electrostatic model considered for charging of the polysilicon grain. The blue box represents an SEB whereas the red box represents an SET. SET and SEB are connected via a capacitor C_{dd} .

aligns with the electrochemical potential (μ_{D2}) of $D2$. Therefore, upon application of a gate bias, the condition required to charge $D2$ with an electron is:

$$\mu_{g0} - eV_g = \frac{(en_2)^2}{C_{\Sigma 2}} - \frac{e\left(C_{S2}V_s + C_{D2}V_d + C_{G2}V_g\right)}{C_{\Sigma 2}} \tag{5.5}$$

Rearranging the equation gives:

$$e\left(\frac{C_{G2}}{C_{\Sigma 2}} - 1\right)V_g = \frac{(en_2)^2}{C_{\Sigma 2}} - \frac{eC_{S2}V_s}{C_{\Sigma 2}} - \frac{eC_{D2}V_d}{C_{\Sigma 2}} - \mu_{g0}$$

For source grounded and bias applied to the drain, we substitute $V_s = 0$ and differentiate the above equation w.r.t V_g gives the slope of the boundary line equation in the $V_g - V_d$ plane:

$$\frac{dV_d}{dV_g} = \frac{C_{D2} + C_{S2}}{C_{D2}} \tag{5.6}$$

This is one of the central results of this chapter.

Capacitor	Capacitance (aF)	Barrier Conductance $\left(\frac{e^2}{h}\right)$
C_{S1}	11.4	0.1
C_{D1}	9	0.1
C_{S2}	80	0
C_{D2}	80	0
C_{G2}	100	0.1
C_{dd}	14	0

Table 5.1: Parameters used for simulation in fig. 5.5.

5.5 Comparison between Electrostatic Model and Measurements

In this section we will compare the measurements with the electrostatic model proposed in the last section.

5.5.1 Single Grain Model

In the previous section the electrostatic model includes a single polysilicon grain in the gate. Although C_{dd} is assumed to be insignificant when considering the charging of the polysilicon grain $(D2)$, it still couples the SET to the SEB. It is due to this coupling capacitor that the effect of charging in $D2$ is seen in the conductance measurements. Eq. 5.6 suggests that for a symmetric capacitive coupling of $D2$ to source and drain a slope of 2 is to be expected for features related to charging of the grain in the gate in the conductance measurement (fig. 5.2), which is indeed observed in the measured data. Hence, we observe the charging of the SEB in the conductance measurements of the SET. Figs. 5.5a and 5.5b show the simulated differential conductance and transconductance for the model shown in fig. 5.4, in good agreement with experimental data shown in figs. 5.2a and 5.2b. The simulation is based upon the master equation technique [74][82]. The parameters used for the simulation are summarized in table 5.1.

The period of the lines with slope 2 is dominated by the capacitive coupling between the $D2$ and source and drain, i.e. C_{S2} and C_{D2}. The period of oscillations in $D1$ is determined by C_{dd} and is given by $\frac{e}{C_{dd}}$. Only conductance lines with positive slopes are visible in the measured and simulated data resulting from the charging of $D2$. This can be explained in terms of the single tunnel barrier connected to $D2$. The charge on $D2$ can fluctuate only when $\mu_g = \mu_{D2}$ which results in conductance lines with positive slopes. The conclusions of this simple model have been confirmed by more detailed simulations which take the capacitive coupling between the SET and the SEB into

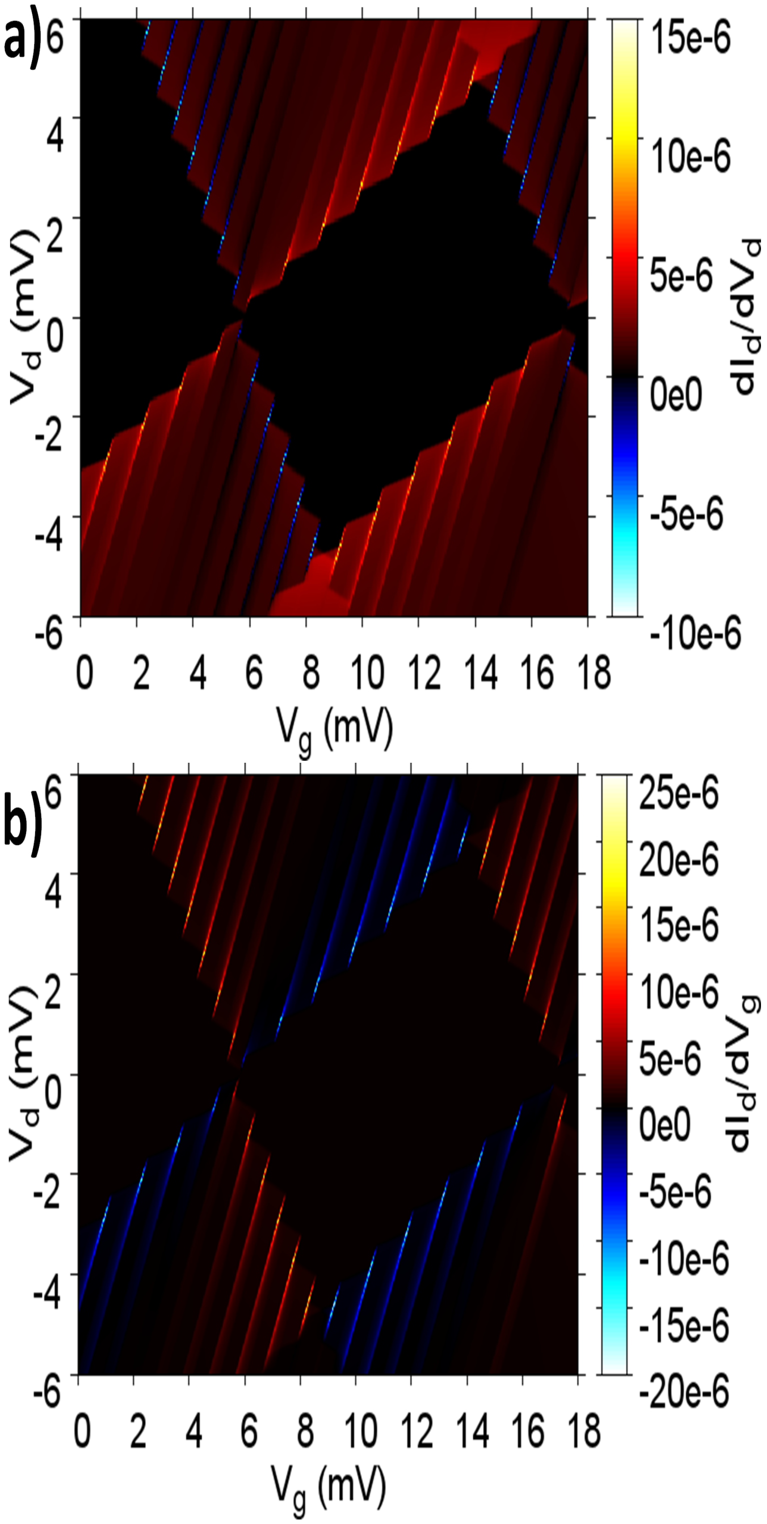

Figure 5.5: a) Simulated differential conductance for the model shown in fig. 5.4. Parameters used for the simulation are given in table 5.1. b) Simulated transconductance with the same parameters.

account. Charging of the polysilicon grain is seen in the conductance measurement if the charging energy of the grain is much larger than the thermal energy.

5.5.2 Origin of Positive and Negative Differential Conductance and Transconductance

Both, the simulations and the detailed measurements show positive (increase in conductance) and negative (decrease in conductance) conductance lines along the edges of the Coulomb diamond. On the one hand, in the differential conductance measurements, the positive and negative conductance lines are seen on positive and negative slopes of the Coulomb diamond, respectively. On the other hand, in the transconductance measurements, the positive and negative conductance lines are seen on negative and positive slopes of the Coulomb diamond, respectively. First, we consider the differential conductance measurements and simulations. The boundaries of a Coulomb diamond with a positive slope correspond to an alignment of the electrochemical potential of $D1$ with the electrochemical potential of the drain. When the charge state of $D2$ is changed discretely, e.g. reduced by one for increasing V_g, due to capacitive coupling between $D1$ and $D2$ this shifts the electrochemical potential of $D1$ within the transport window. This shift of electrochemical potential results in enhancing the current. Therefore, lines of positive differential conductance are observed along the positive slope of the Coulomb diamond. Similarly, for a negative slope of the Coulomb diamond, the electrochemical potential of the $D1$ aligns with the electrochemical potential of the source. When the charge state of $D2$ changes discretely, this pushes the electrochemical potential of $D1$ outside the transport window. This shift of electrochemical potential results in supression of the current. Therefore, lines of negative differential conductance are observed along the negative slope of the Coulomb diamond. The simulation result for differential conductance is shown in fig. 5.5a.

To explain the origin of positive and negative transconductance lines in the transconductance measurements we consider fig. 5.6a which shows simulated transconductance of a quantum dot tunnel coupled to source and drain and capacitively coupled to the gate in the non-linear regime. From the simulated data we can see that in the vicinity of a negative slope edge there is positive transconductance and in the vicinity of a positive slope edge there is negative transconductance. Let us consider a point A in the vicinity of a negative slope as shown in fig. 5.6a. When $D2$ is charged discretely, this shifts the electrochemical potential on $D1$ to lower gate voltage. This shift in electrochemical potential results in going from a region of low positive transconductance to a region of high positive transconductance. This results in a net positive transconductance. Fig. 5.6b (top) shows the surface plot of the simulated transconductance based on the model shown in fig. 5.4 in the non-linear regime and fig. 5.6b (bottom) shows the same data as in fig. 5.6b (top) in 2-D color plot. In fig. 5.6b (bottom) yellow line indicates the negative slope of the Coulomb diamond due to $D1$ in fig. 5.4. From the surface plot in fig. 5.6b (top), we can see that everytime $D2$ is charged in the vicinity of a negative slope, we see a net positive transconductance. This gives rise to positive transconductance lines as seen in fig. 5.6 (bottom). Similarly, we consider a point B in the vicinity of a positive slope as shown in fig. 5.6a. When $D2$ is charged

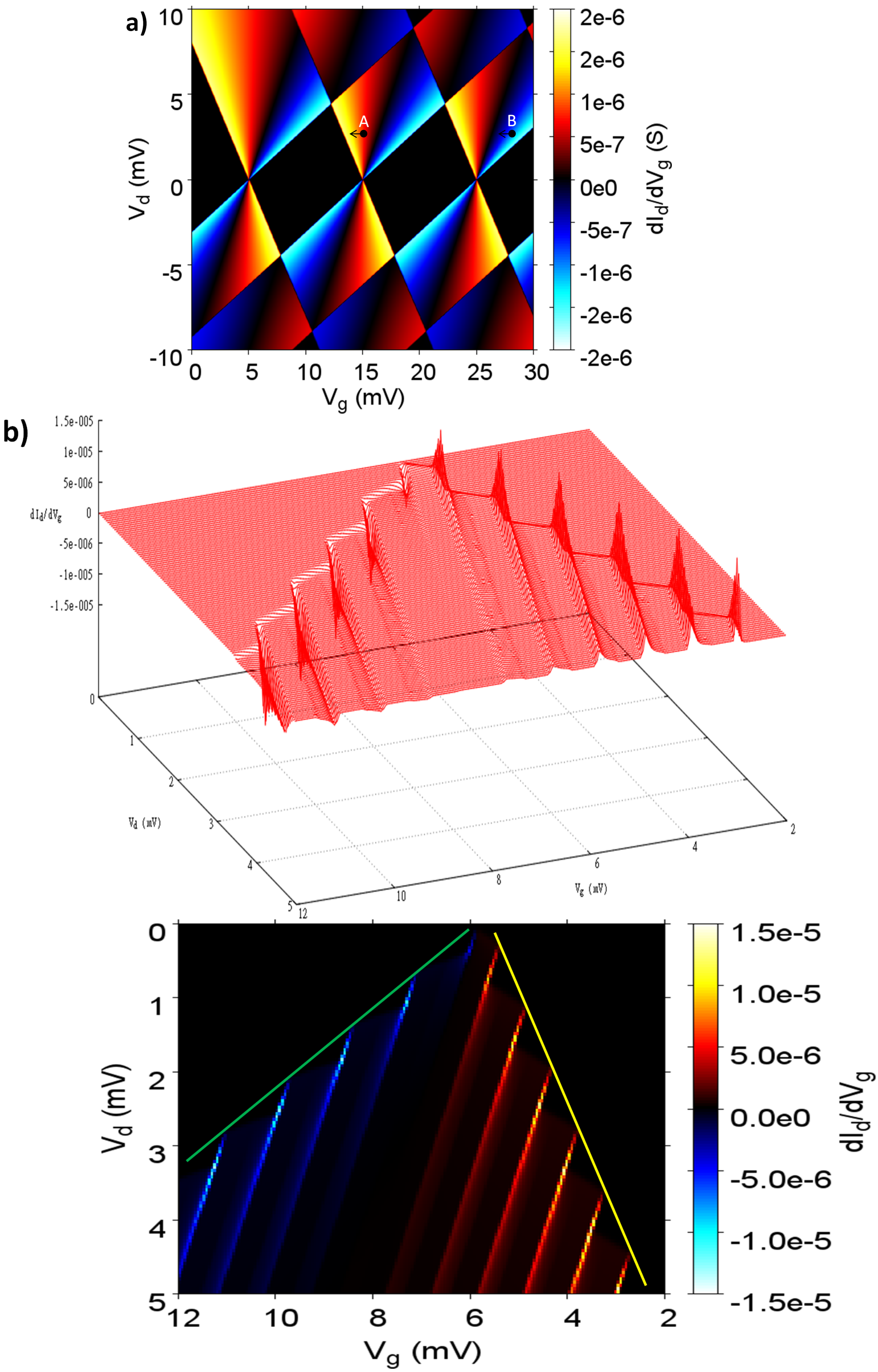

Figure 5.6: a) Simulated transconductance of a single quantum dot tunnel coupled to source and drain and capacitively coupled to gate in the non-linear region. b) Above: Surface plot of small range in fig. 5.5b. Bottom: 2-D plot fig. 5.6b (Above).

discretely, this shifts the electrochemical potential on $D1$ again to lower gate voltage. This shift in electrochemical potential results in going from a region of high negative conductance to a region of low negative conductance. In the fig. 5.6b (bottom) green line indicates a positive slope of the Coulomb diamond due to $D1$in fig. 5.4. From the surface plot in fig. 5.6b (top), we can see that everytime $D2$ is charged in the vicinity of a positive slope, we see a net negative transconductance. This gives rise to negative transconductance lines as seen in fig. 5.6 (bottom).

In the measurements and simulations near $V_d = 0$ a non-conducting region is seen marked by a circle in fig. 5.2a. When the electrochemical potential of $D1$ aligns with the electrochemical potential of the source and drain (in the limit of linear response) a Coulomb peak appears. The complete supression of the current at zero V_d is seen when an electron tunnels from $D2$ to the gate electrode. An electron tunneling from $D2$ to gate shifts the electrochemical potential of $D2$. Since $D1$ and $D2$ are capacitively coupled, electrochemical potential of $D1$ is also shifted. This brings the electrochemical potential of $D1$ and source and drain out of alignment bringing $D1$ back into blockade region. Such charging events taking place in a small voltage range can lead to non-conducting region near $V_d = 0$.

5.5.3 Multi-grain Model

In the previous subsection only a single grain was considered in the polysilicon gate which coupled to $D1$ capacitively. Charging effects in the polysilicon grain can be seen if it satisfies both the conditions in eq. 5.1 and eq. 5.2. An electrostatic model was considered with a single polysilicon grain ($D2$) capacitively coupled to $D1$ and symmetrically capacitively coupled to source and drain. In real devices there can be more than one polysilicon grain which can get charged and may not always be symmetrically capacitively coupled to source and drain (fig. 5.7). If the grains are asymmetrically coupled to source and drain then, according to eq. 5.6 the slope of the lines due to charging of a polysilicon grain also deviates from 2. Furthermore, looking at the high resolution measurements in fig. 5.8a we can see that these conductance lines are not periodic. This aperiodicity cannot be explained with a single grain in the polysilicon gate. Hence, a model is proposed with more than one polysilicon grain being charged in the polysilicon gate. Here we consider an electrostatic model with two polysilicon grains in the gate. The electrostatic model is shown in fig. 5.7. In the model, the dots $D1$, $D2$ and $D3$ are considered in parallel. Dot $D3$ is tunnel-coupled to the gate and capacitively coupled to source, drain, $D1$ and $D2$. Similarly, $D2$ is tunnel-coupled to the gate and capacitively coupled to source, drain, $D1$ and $D3$. This is one of the several possible configurations which can generate aperiodic conductance lines. Also, in the electrostatic model in fig. 5.7, only two grains are considered in the gate for simplicity, but in real devices there can be more than two grains with a large number of possible configurations. Fig. 5.8b shows the result of the simulation of conductance in the non-linear regime for the configuration shown in fig. 5.7. The parameters used for the simulation are summarized in the table 5.2. Fig. 5.9a shows the transconductance measurement on a type B (fig. 5.1) sample at $4.2K$. It shows lines which are aperiodic and have different slopes. A typical spacing of these lines is $\sim 15mV$. Comparing the

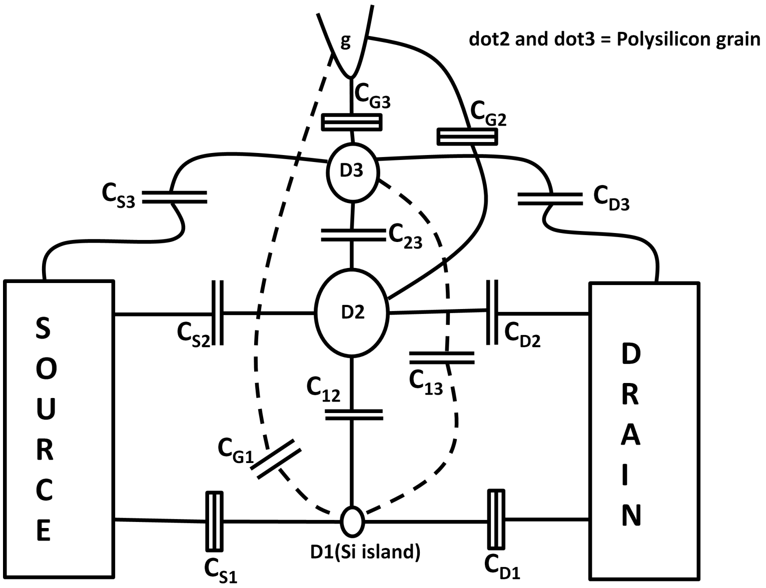

Figure 5.7: Electrostatic model for multi-grain charging in the polysilicon gate.

transconductance measurements in fig. 5.9a and in fig. 5.2, we can conclude that the size of the polysilicon grain getting charged is much smaller than the one in the fig. 5.2. The lines with slope > 1 in fig. 5.2 are not visible at $T = 4.2K$, possibly due to the thermal energy being higher than the charging energy of the polysilicon grain in the gate while in fig. 5.9a they are clearly visible. The red, green and blue lines in fig. 5.9a correspond to a slope of 1.3, 2 and 3.4, respectively. This supports the previous assumption of more than one grain in the polysilicon gate being charged and coupled asymetrically to the electrodes source, drain and gate. The slope of 2 is due to symmetric capacitive coupling of the polysilicon grain to source and drain while slopes of 1.3 and 3.4 are due to asymmetric capacitive coupling. From eq. 5.6 slopes < 2 are expected when the capacitive coupling from the drain to the polysilicon grain is dominant while slopes > 2 are expected when the capacitive coupling from the source to the polysilicon grain is the dominant one. This condition can be summarized as follows:

$$
\begin{aligned}
\frac{C_{D2}+C_{S2}}{C_{D2}} &= 2\ if\ C_{D2} = C_{S2} \\
&< 2\ if\ C_{D2} > C_{S2} \\
&> 2\ if\ C_{D2} < C_{S2}
\end{aligned}
\tag{5.7}
$$

If $C_{D2} \gg C_{S2}$, eq. 5.6 predicts a slope of close to 1 whereas if $C_{S2} \gg C_{D2}$, eq. 5.6 predicts a slope of ∞. Fig. 5.9b shows the differential conductance measurment at $4.2K$. We see that there are charging lines which run perpendicular to the $V_g - axis$. This is the result of $C_{S2} \gg C_{D2}$.

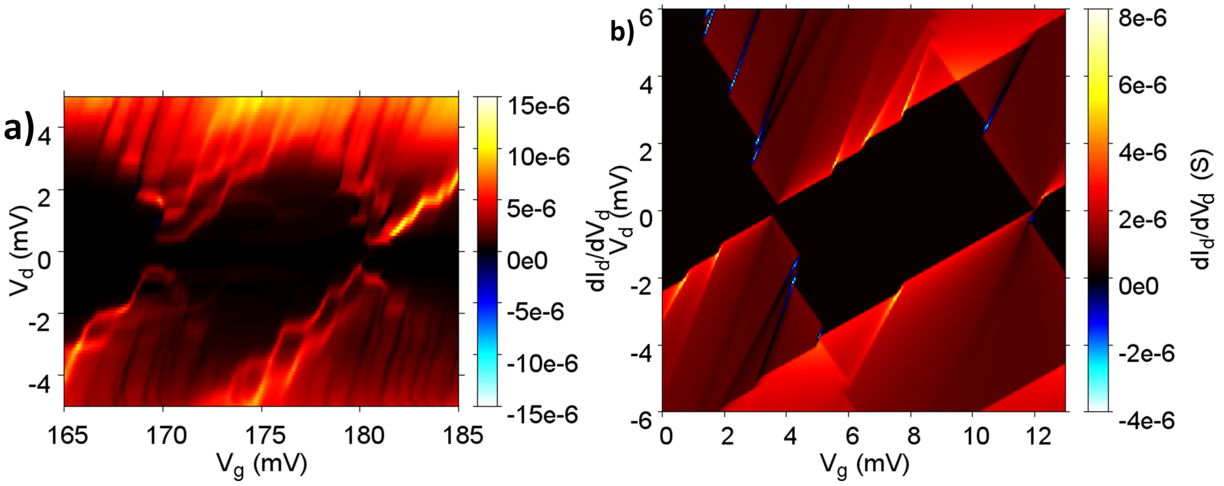

Figure 5.8: a) High resolution differential conductance measurement at $T = 70mK$ showing lines with slope > 1. These lines are aperiodic. b) Simulated differential conductance based on the model shown in fig. 5.7. Simulated data shows aperiodic lines with different slopes validating the assumption of multi-grain charging in the polysilicon gate. Parameters used in the simulation are summarized in table 5.2.

Capacitor	Capacitance (aF)	Barrier Conductance ($\frac{e^2}{h}$)
C_{S1}	11.4	0.1
C_{D1}	9.2	0.1
C_{S2}	60	0
C_{D2}	40	0
C_{S3}	15	0
C_{D3}	23	0
C_{G2}	100	0.1
C_{G3}	100	0.1
C_{G1}	7	0
C_{13}	6	0
C_{23}	8	0
C_{12}	9	0

Table 5.2: Parameters used for simulation. The result of the simulation is shown in fig. 5.8b.

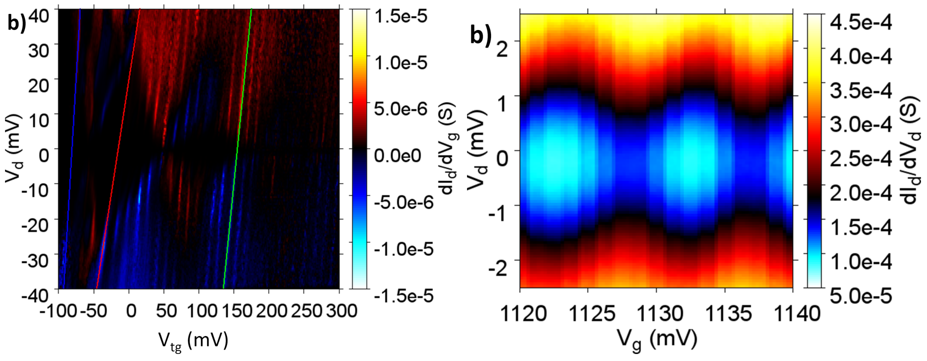

Figure 5.9: a) Transconductance measurement at $4.2K$ for a device with dimensions $L = 40nm$, $W = 20nm$, $Tsi = 20nm$ and $t_{spacers} = 40nm$. Lines with slope > 1 are clearly visible due to charging effects in the polysilicon gate. The red, green and blue lines correspond to slopes of 1.3, 2 and 3.4, respectively due to multi-grain charging in the polysilicon. Different grains exhibit different coupling to source, drain and gate. b) Differential conductance measurement at $T = 4.2K$ for a device with similar dimensions as in a) demonstrating the case $C_{S2} \gg C_{D2}$ which results in charging lines running perpendicular to the $V_g - axis$.

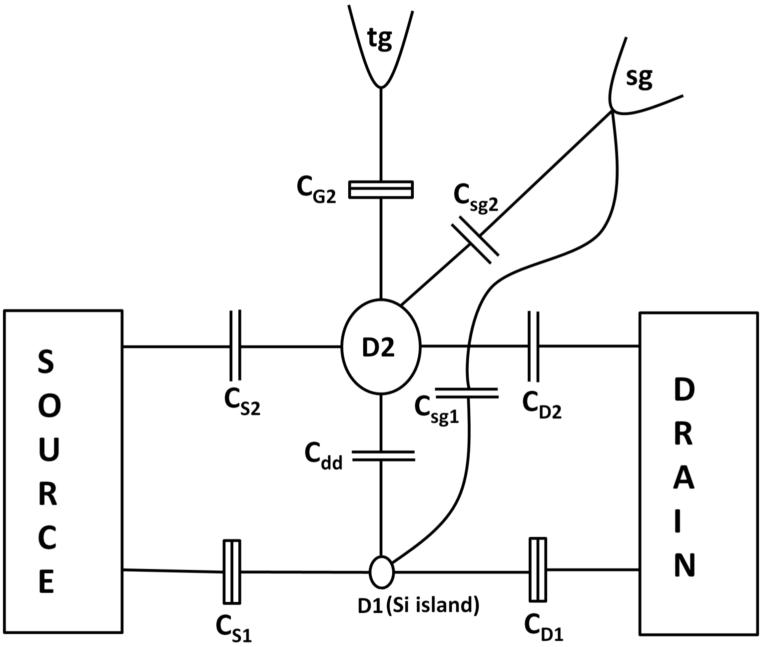

Figure 5.10: Electrostatic model considered for the device with side gate geometry.

5.6 Conductance Measurement as a Function of Side Gate in Linear Regime

Using the sidegate geometry of the type B devices, it is possible to study the electron transport through the silicon dot in the linear regime. Fig. 5.9a shows the non-linear response of this device, where clearly lines with slope > 1 are visible. Using the side gate geometry, we investigate the transport properties in the linear regime. With the polysilicon grain in the gate behaving as the second quantum dot, the device has a parallel dot configuration. Unlike in the serial configuration, electrons are added to each dot independent of each other. As a result, transport occurs along some of the lines that connect the triple points, which we call charging lines (Coulomb oscillations) in the following. Fig. 5.10 shows the electrostatic model for the device under consideration. In fig. 5.10, only one side gate is considered since conductance is studied as a function of top gate vs one of the side gates (either side gate 1 while side gate 2 is grounded or vice versa).

Fig. 5.11a shows the differential conductance measurement as a function $V_{tg} - V_{sg2}$. Fig. 5.11a (right) shows the magnified region in fig. 5.11a (left). We can see two types of charging lines in fig. 5.11a (right). One charging line is marked by black solid line which has a negative slope. We attribute this to charging of the quantum dot in the silicon nanowire denoted by $D1$ in fig. 5.10. This conclusion arise from the fact that an island tunnel coupled to source and drain and capacitively coupled to two gates generates charging line with negative slope in the $V_{tg} - V_{sg2}$ space. The slope of the charging line depends on the ratio of capacitive coupling betweeen the island and the two gates. The period of oscillations due to $D1$ as a function of V_{tg} and V_{sg2} is $\sim 12.5mV$ and $\sim 200mV$, respectively. The second charging line is indicated by red dotted line in fig. 5.11a (right) which has a positive slope. The slope of second charging line is unusual since an island tunnel coupled to either source or drain or

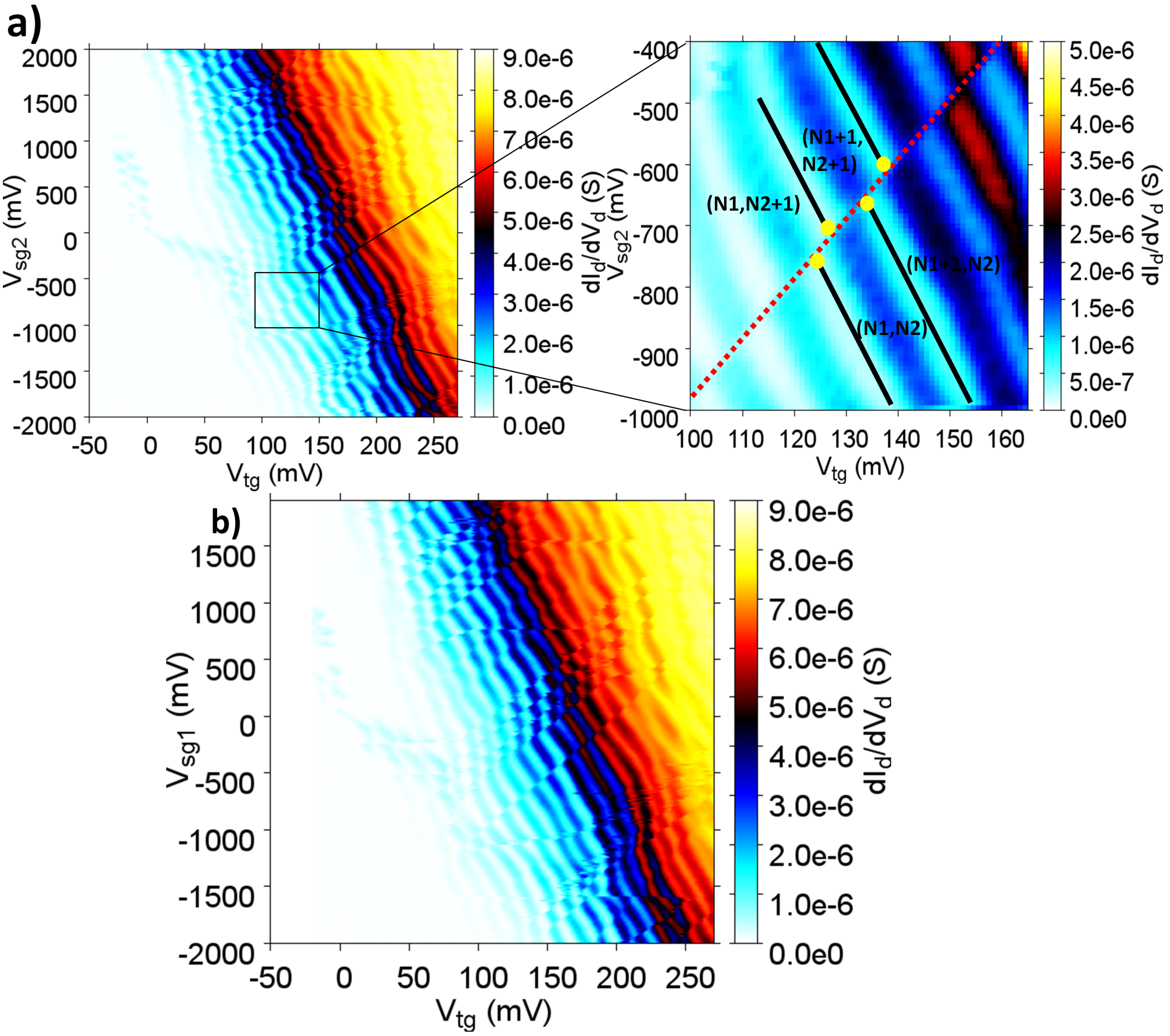

Figure 5.11: a) Left: Differential conductance measurement at 4.2K as a function of top gate and the side gate2. Right: Magnified region of a). b) Differential conductance measurement at 4.2K as a function of top gate and the side gate1.

Capacitor	Capacitance (aF)	Barrier conductance $\left(\frac{e^2}{h}\right)$
C_{G11}	10	0
C_{G12}	1	0
C_{G13}	0.8	0
C_{G21}	10	0.1
C_{G22}	15	0.1
C_{S3}	20	0.1
C_{D3}	20	0.1
C_{13}	20	0
C_{23}	5	0

Table 5.3: Parameters used for simulation in fig. 5.12.

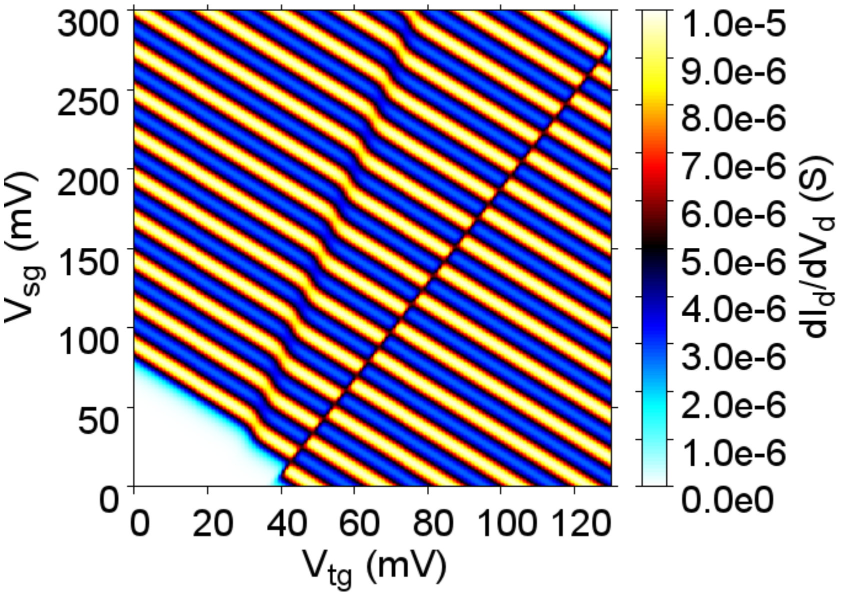

Figure 5.12: Simulated differential conductance showing charging lines with positive slope as seen in the measurements in fig. 5.11.

another island always generates charging line with negative slope. We attribute this charging line to charging of the polysilicon grain in the top gate. The charging of the polysilicon grain indicates that with increase in gate voltage (top gate or the side gate) the electrochemical potential in the polysilicon grain $(D2)$ is raised which results in positive slope in $V_{tg} - V_{sg2}$ space. This supports our previous arguement in section 5.5.2 that when electrochemical potential in $D2$ aligns with the electrochemical potential in the V_{tg} an electron tunnels from $D2$ to V_{tg}. This raises the electrochemical potential in the $D2$ resulting in positive slope with increase in gate voltage. Similar charging lines are seen with postive slope in $V_{tg} - V_{sg1}$ space (fig. 5.11b). The period of oscillations due to $D1$ as a function of V_{sg1} is $\sim 300mV$. The yellow solid points in fig. 5.11a (right) indicate the triple points. The charging sequence of the double dot system is shown in fig. 5.11a (right). Based on the electrostatic model in fig. 5.10, simulations were performed. Fig. 5.12 shows simulated conductance data which shows a charging line for $D2$ with positive slope as expected from the electrostatic model and agrees with the measured data. The parameters used are summarized in table 5.3.

Fig. 5.13a shows the transconductance measurement where a small ac voltage is applied to the V_{tg}. The transconductance measurement clearly shows the charging line with a positive slope which is also seen in the differential conductance measurement. In addition, there are also lines with different slopes and with a different period which are due to several grains in the polysilicon gate getting charged. These polysilicon grains have a different capacitive coupling to the gates. Fig. 5.13b shows simulated transconductance data which agree well with the measured data. The parameters used for the transconductance simulation are same as in table 5.3. To conclude, we have studied charging of polysilcion grain in the gate in linear and non-linear regime. We propose an electrostatic model and perform simulations based on this model which explains the measured data very well.

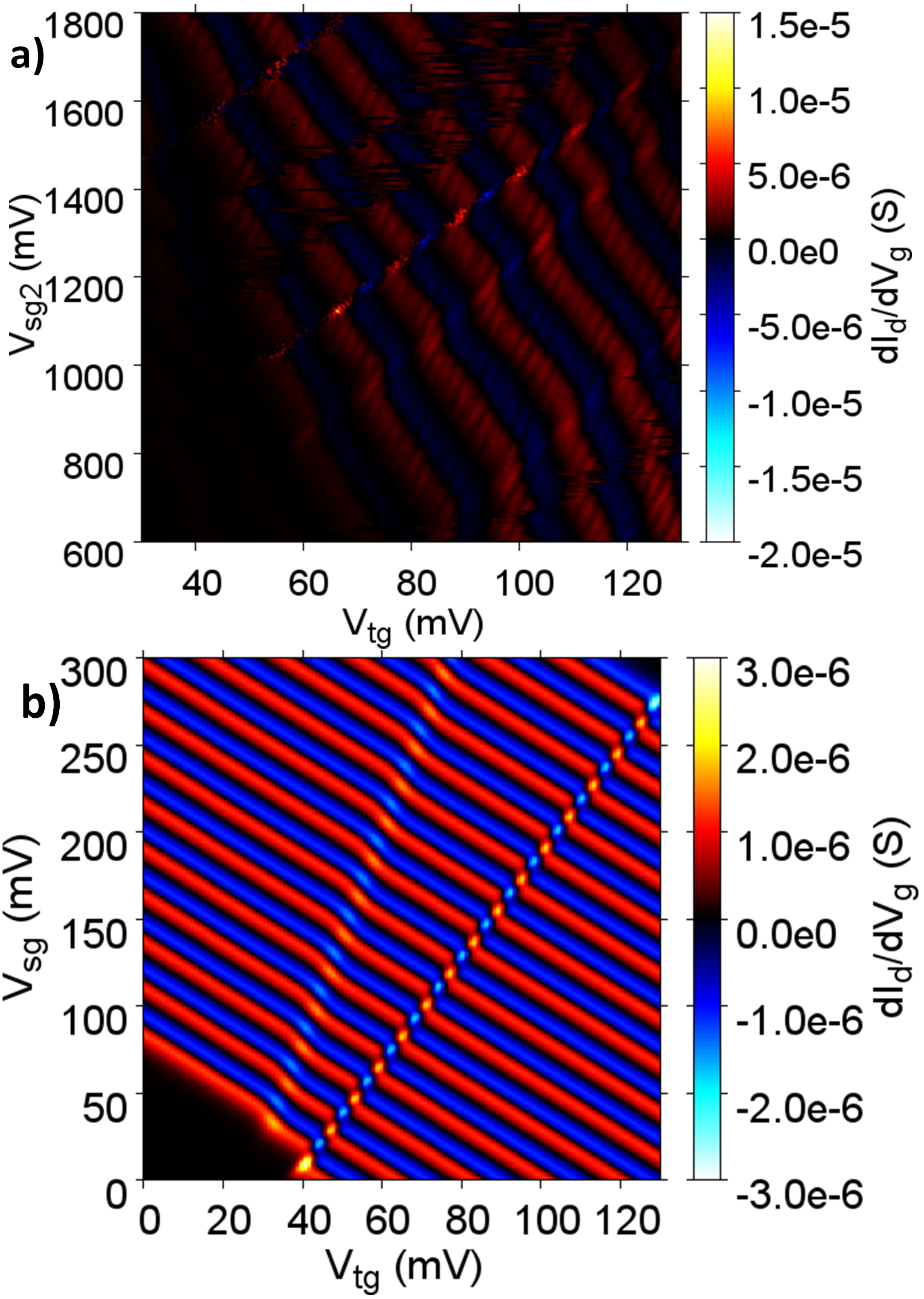

Figure 5.13: a) Transconductance measurement at 4.2*K* of the same device as in fig. 5.11. b) Simulated transconductance generating similar features as seen in a).

Chapter 6

Conclusion

6.1 Overview

In this work, Coulomb blockade in gated silicon nanowires is studied. The devices are fabricated on a CMOS platform taking advantage of advanced silicon technology. The samples were fabricated at CEA, Leti. All the devices which worked at room temperature also worked at low temperature, except those damaged by improper handling or accidental application of high voltages.

A quantum dot in the device is formed by doping gradient and gate voltages, instead of oxide barriers or constrictions. The region below the gate is undoped which forms the quantum dot upon application of a positive gate voltage whereas the region below the spacers, being lowly doped, forms the barriers which separate the quantum dot from the electron reservoirs, the source and the drain. The gate also controls the barriers. Thanks to the state-of-the-art fabrication, device dimensions as small as $20nm$ were fabricated. With the device dimensions on these scale quantum dots with charging energies as high as $40meV$ were achieved which corresponds to thermal energy of $\sim 465K$. Emperically Coulomb charging effects are visible for temperatures $k_BT < 0.3\frac{e^2}{C_\Sigma}$, where C_Σ is the total capacitance of the quantum dot. Hence for the device with charging energy of $40meV$ Coulomb charging effects can be seen upto temperature $T = 140K$. With such a small size of quantum dots, clear excited states were visible even at a temperature as high as $4.2K$.

Putting two single gate devices in close vicinity allowed to study the interaction between the quantum dots. Each dot was formed below the gate and the region between the two dots acts as a barrier. This barrier is controlled by the gates and hence, the coupled dot system was operated in different regimes. The devices could be tuned from weakly tunnel-coupled (ionic bond) to strongly tunnel-coupled (covalent bond). In such devices, optimising the silicon nitride spacers allowed control of the number of dots formed in the device. In devices with large spacers, the region of channel between gates is covered during HDD. This results in formation of just two dots, each below the gate and the region between the dots acts as a barrier. In the devices with small spacers the region of the channel between the two gates remains uncovered. This allows the formation of the third dot. Small spacers with two gates form a compact device where three dots are tuned with just two gates.

Using the side gate geometry, it was possible to study the interaction of the quantum dot (intentionally formed) with its background (unintentionally formed quantum dots).

Charging effects were observed in polysilicon gates. These charging events were detected by the single electron trasistor. This compact device with a single electron box coupled to a single electron transistor shows novel features and is reminiscent of floating dots in memory devices.

6.2 Outlook

We have shown that very good single electon transistors can be formed in silicon nanowires and we have studied the region below the gate which forms the quantum dots. This work aimed at implementing single electron transistors as a future option to replace metal oxide semiconductor field effect transistor, but there are certain issues that still remain unsolved. Variability still remains the key issue due to uncontrolled dopants diffusing into the barriers and the channel. Devices exhibiting Coulomb charging effects at temperatures well beyond $4.2K$ are achieved. This is very encouraging, since our devices are fabricated on a large scale with several hundred devices on each wafer. This opens up the possibility of single electron transistors working at higher temperature produced on a large scale. The issue of variablitly can be addressed by the experience gained in this project. One of the solutions could be to make clean junctions (barriers) by using steep dopant concentration gradient. This may be useful to reduce the number of dopants in the barriers and improve the device performance over the present situation.

Bibliography

[1] International Technology Roadmap for Semiconductors: Reports. URL http://www.itrs.net/reports.html.

[2] K. K. Likharev, Single-Electron Devices and Their Applications, Proceedings of the IEEE Vol. 87 Issue 4, 606-632, April (1999),

[3] H. Grabert and M. H. Devoret (editors), Single Charge Tunneling – Coulomb Blockade Phenomena in Nanostructures, volume 294 of NATO ASI series B: Physics. Plenum Press (1992), p.1-21.

[4] M. Hofheinz, X. Jehl, M. Sanquer, G. Molas, M. Vinet, and S. Deleonibus, Simple and controlled Single Electron Transistor based on Doping Modulation in Silicon Nanowires, Appl. Phys. Lett. 89, 143504 (2006).

[5] G. Feher, Electron spin resonance experiments on donors in silicon. I. Electronic structure of donors by the electron nuclear double resonance technique. Phys. Rev. 114, 1219–1244 (1959).

[6] G. Feher and E. A. Gere, Electron spin resonance experiments on donors in silicon. II. Electron spin relaxation effects. Phys. Rev. 114, 1245–1256 (1959).

[7] Atomic functionalities on Silicon devices. http://www.afsid.eu/

[8] C. J. Gorter, A possible explanation of the increase of the electrical resistance of thin metal films at low temperatures and small field strengths, Physica, Vol. 17 Issue 8, August 1951, 777-780.

[9] I. Giaver and H. R. Zeller, Superconductivity of small tin particles measured by tunneling, Phys. Rev. Lett. 20, 1504-1507 (1968).

[10] P. Sheng, B. Abeles, and Y. Arie, Hopping Conductivity in Granular Metals, Phys. Rev. Lett. 31 , 44-47(1973).

[11] L. L. Sohn, L. P. Kouwenhoven, and G. Schön (edited by), Mesoscopic electron transport, NATO ASI series, Series-E: Applied Sciences-Vol.345, p.105-214 (1997).

[12] T. Ando, Y. Arakawa, and K. Furuya, Mesoscopic physics and electronics, Nanoscience and Technology, Springer (1998).

[13] Zahid Ali Khan Durrani, Single-Electron Devices and Circuits in Silicon, Imperial College Press (2010).

[14] Michel H. Devoret, Daniel Esteve & Cristian Urbina, Single-electron transfer in metallic nanostructures, Nature 360, 547 - 553 (10 December 1992).

[15] Lafarge, P. et al. Direct observation of macroscopic charge quantization, Z. Phys. B 85, 327-332 (1991).

[16] Geerligs et al., Frequency-locked turnstile device for single electrons. Phys. Rev. Lett. 64, 2691–2694 (1990).

[17] H. Nakazato, R.J. Blaikie, H. Ahmed, Single-electron memory, J. Appl. Phys., 75 (10) (1994), pp. 5123–5134.

[18] Grabert H., Ingold G. L., Devoret M.H., Esteve D., Pothier H. and Urbina C, Single electron tunneling rates in multijunction circuits. Z. Phys. B 84: 143–155 (1991).

[19] K. K. Likharev, Single-electron devices and their applications. Proceedings of the IEEE, Vol 87 Issue 4, 606–632 (1999).

[20] Fulton T.A. and Dolan G.J., Observation of single-electron charging effects in small tunnel junctions, Phy. Rev. Lett. 59, 109–112 (1987).

[21] Likharev K.K. Correlated discrete transfer of single electrons in ultrasmall tunnel junctions. IBM J. Res. Develop 32, 144–158 (1988).

[22] Michael Tinkham, Introduction to Superconductivity, McGraw Hill, Inc. (1996).

[23] Thomas Ihn, Semiconductor Nanostructures Quantum States and Electronic Transport, Oxford University Press (2010).

[24] Beenakker C.W.J., Theory of Coulomb-blockade oscillations in the conductance of a quantum dot, Phys. Rev. B 44, 1646–1656 (1991).

[25] A. Tilke et al., Coulomb blockade in Silicon nanostructures, Progress in Quantum Electronics, Vol.25 (2001), p.97.

[26] R. Nuryadi, Master Equation-Based Numerical Simulation in a Single Electron Transistor, in J. Awrejcewicz (edited by), Numerical Simulations of Physical and Engineering Processes, p. 239-256, InTech (2011).

[27] Reed M.A. et. al., Observation of discrete electronic states in a zero-dimensional semiconductor nanostructure. Phys. Rev. Lett. 60, 535–537 (1988).

[28] Kastner, M. A., Artificial Atoms, Physics Today ,Volume 46 Issue 1, 24–31 (1993).

[29] John H. Davies, The Physics of Low Dimension Semiconductors, Cambridge University Press (1998).

[30] M. Hofheinz, X. Jehl, and M. Sanquer G. Molas, M. Vinet, and S. Deleonibus, Capacitance enhancement in Coulomb blockade tunnel barriers , Phys. Rev. B 75, 235301 (2007).

[31] X. Jehl et.al., Mass Production of Silicon MOS-SETs: Can We Live with Nano-Devices' Variability?, Procedia Computer Science 7 (2011) 266–268.

[32] Enrico Parti et.al., Few electron limit of n-type metal oxide semiconductor single electron transistors, Nanotechnology, Volume 23, Issue 21, pp. 215204 (2012).

[33] G.Molas, PhD. Thesis, CEA Leti, Grenoble 2004.

[34] Akira Fujiwara et. al., Single electron tunneling transistor with tunable barriers using silicon nanowire metal-oxide-semiconductor field-effect transistor, Appl. Phys. Lett. 88, 053121 (2006).

[35] Hymer Hybond 472A Manual.

[36] H. London, Proceedings of the International Conference on Low-Temperature Physics, Oxford University Press (1951).

[37] F. Pobell, Matter and Methods at Low Temperatures, Springer-Verlag, 1992.

[38] Nathaniel Craig and Ted Lester, Hitchhiker's Guide to the Dilution Refrigerator (2004).

[39] National High Magnetic Field Laboratoray, ULR: http://www.magnet.fsu.edu/education/tutorials/tools/dilutionfridge.html

[40] M. Hofheinz, Coulomb blockade in Silicon Nanowire MOSFETs, PhD. Thesis, CEA Leti, Grenoble 2006.

[41] B. Zeghbroeck, Principles of Electronic Devices (2011). ULR: http://ecee.colorado.edu/~bart/book/

[42] Pothier, H., P. Lafarge, C. Urbina, D. Estève, and M. H. Devoret, Single-Electron Pump Based on Charging Effects, Europhys. Lett. 17, 249 (1992).

[43] Ruzin, I. M., V. Chandrasekhar, E. I. Levin, and L. I. Glazman, Stochastic Coulomb blockade in a double-dot system, Phys. Rev. B 45, 13469 (1992).

[44] W.G. van der Wiel, S. De Franceschi, J.M. Elzerman, T. Fujisawa, S. Tarucha, L.P. Kouwenhoven, Electron transport through double quantum dots, Rev. Mod. Phys. Vol. 75 No. 1, 1-22 (2003).

[45] Cohen-Tannoudji, C., B. Diu, and F. Laloë, Quantum Mechanics, Volume one, John Wiley & Sons (1977).

[46] H. Qin et.al., Probing coherent electronic states in double quantum dots, phys. stat. sol. (c) 1, No. 8, 2094–2110 (2004).

[47] M. Hofheinz, X. Jehl, M. Sanquer, G. Molas, M. Vinet, S. Deleonibus, Individual charge traps in silicon nanowires: Measurements of location, spin and occupation number by Coulomb blockade spectroscopy, Euro. Phys. J. B 54, 299-307 (2006).

[48] M. R. Gräber et.al., Molecular states in carbon nanotube double quantum dots, Phys. Rev. B 74, 075427 (2006).

[49] R. H. Blick, D. Pfannkuche, R. J. Haug, K. v. Klitzing, and K. Eberl, Formation of a Coherent Mode in a Double Quantum Dot, Phys. Rev. Lett. 80, 4032–4035 (1998).

[50] M. A. Kastner, The single-electron transistor, Rev. Mod. Phys. 64, 849–858 (1992).

[51] R. Augke, W. Eberhardt, C. Single, F.E. Prins, D.A. Wharam, D.P. Kern, Appl. Phys. Lett. 76 (2000) 2065.

[52] F. Hofmann, T. Heinzel, D. Wharam, J. Kotthaus, G. Böhm, W. Klein, G. Tränkle, and G. Weimann, Single electron switching in a parallel quantum dot, Phys. Rev. B 51, 13872 (1995).

[53] J. M. Elzerman, R. Hanson, J. S. Greidanus, L. H. W.van Beveren, S. D. Franceschi, L. M. K. Vandersypen, S. Tarucha, and L. P. Kouwenhoven, Few-electron quantum dot circuit with integrated charge read out, Phys. Rev. B 67, 161308 (2003).

[54] C Single, R Augke, F E Prins, D A Wharam and D P Kern, Single-electron charging in doped silicon double dots, Semicond. Sci. Technol. 14 (1999) 1165–1168.

[55] Alexander N. Korotkov and Konstantin K. Likharev, Single-electron-parametron-based logic devices, J. Appl. Phys. 84, 6114 (1998).

[56] M. Stopa, Rectifying Behavior in Coulomb Blockades: Charging Rectifiers, Phys. Rev. Lett. 88, 146802 (2002).

[57] C. Single, R. Augke, F.E. Prins, D.A. Wharam, D.P. Kern, Towards quantum cellular automata operation in silicon: transport properties of silicon multiple dot structures, Superlattices and Microstructures 28, 429 (2000).

[58] F. R. Waugh, M. J. Berry, D. J. Mar, R. M. Westervelt, K. L. Campman, and A. C. Gossard, Single-Electron Charging in Double and Triple Quantum Dots with Tunable Coupling, Phys. Rev. Lett. 75, 705 (1995).

[59] D. Schroer, A. D. Greentree, L. Gaudreau, K. Eberl, L. C. L. Hollenberg,J. P. Kotthaus, and S. Ludwig, Electrostatically defined serial triple quantum dot charged with few electrons, Phys. Rev. B 76, 075306 (2007).

[60] A. Vidan, R. M. Westervelt, M. Stopa, M. Hanson, and A. C. Gossard, Triple quantum dot charging rectifier, Appl. Phys. Lett. 85, 3602 (2004).

[61] M. Pierre, R. Wacquez, B. Roche, X. Jehl, M. Sanquer, M. Vinet, E. Prati, M. Belli, and M. Fanciulli, Compact silicon double and triple dots realized with only two gates Appl. Phys. Lett. 95, 242107 (2009).

[62] S. D. Lee, K. S. Park, J. W. Park, J. B. Choi, S. R. E. Yang, K. -H. Yoo, J. Kim, S. I. Park, and K. T. Kim, Single-electron spectroscopy in a coupled triple-dot system: Role of interdot electron-electron interactions, Phys. Rev. B 62, R7735 (2000).

[63] Ke Xu, Jonathan E. Green,‡J. R. Heath, F. Remacle and R. D. Levine, The Emergence of a Coupled Quantum Dot Array in a Doped Silicon Nanowire Gated by Ultrahigh Density Top Gate Electrodes, J. Phys. Chem. C (2007), 111, 17852-17860.

[64] L. I. Glazmann and V. Chandrashekar, Coulomb Blockade Oscillations in a Double-Dot System, Europhys. Lett. 19 623 (1992).

[65] R. Augke, W. Eberhardt, C. Single, F. E. Prins, D. A. Wharam, and D. P. Kern, Doped silicon single electron transistors with single island characteristics, Appl. Phys. Lett. 76, 2065 (2000).

[66] M. Manoharan, Shunri Oda and Hiroshi Mizuta, Impact of channel constrictions on the formation of multiple tunnel junctions in heavily doped silicon single electron transistors, Appl. Phys. Lett. 93, 112107 (2008).

[67] K. Yano, T. Ishii, T. Hashimoto, T. Kobayashi, F. Murai, and K.Seki, Transport characteristics of polycrystalline-silicon with influenced by single electron charging at room temperature, Appl. Phys. Lett., vol. 67, no. 6, pp. 828–830 (1995).

[68] Andrew C. Irvine, Zahid A. K. Durrani, Haroon Ahmed and Serge Biesemans, Single-electron effects in heavily doped polycrystalline silicon nanowires, Appl. Phys. Lett. 73, 1113 (1998).

[69] W. Neu, R. Augke, F.E. Prins, D.P. Kern, Coulomb-blockade-structures in polycrystalline silicon, Microelectronic Engineering 57–58 (2001) 989–993.

[70] J.H.F Scott-Thomas, S. B. Field, M. A. Kastner, H. I. Smith and D.A Antoniadia, Conductance Oscillations Periodic in the Density of a One-Dimensional Electron Gas, Phys. Rev. Lett. 62, 583–586 (1989).

[71] Hideyuki Matsuoka, Tsuneo Ichiguchi, Toshiyuki Yoshimura, and Eiji Takeda, Coulomb blockade in the inversion layer of a Si metal oxide semiconductor field effect transistor with a dual gate structure, Appl. Phys. Lett. 64, 586 (1994).

[72] F. Boeuf, X. Jehl, M. Sanquer, T. Skotnicki, Controlled single-electron effects in nonoverlapped ultra-short silicon field effect transistors, IEEE transactions on Nanotechnology, vol.12 No.3, p.144 (2003).

[73] K. K. Likharev, Correlated discrete transfer of single electrons in ultrasmall junctions, IBM J. Res. Dev. 32, 144 (1988).

[74] M. Pierre, M. Hofheinz, X. Jehl, M. Sanquer, G. Molas, M. Vinet, S. Deleonibus, Background charges and quantum effects in quantum dots transport spectroscopy, Eur. Phys. J. B 70, 475-481 (2009).

[75] C. C. Escott, F. A. Zwanenburg and A. Morello, Resonant tunnelling features in quantum dots, Nanotechnology 21, 274018 (2010).

[76] Dietmar Weinmann, Wolfgang Häusler, and Bernhard Kramer, Spin Blockades in Linear and Nonlinear Transport through Quantum Dots, Phys. Rev. Lett. 74, 984–987 (1995).

[77] Bhaskaran Muralidharan and Supriyo Datta, Generic model for current collapse in spin-blockaded transport, Phys. Rev. B 76, 035432 (2007).

[78] T. Schmidt, R.J. Haug, Vladimir I. Fal'ko, K. v. Klitzing, A. Förster and H. Lüth, Observation of the Local Structure of Landau Bands in a Disordered Conductor, Phys. Rev. Lett. 78, 1540–1543 (1997).

[79] J. Koenemann, P. Koenig, T. Schmidt, E. McCann, Vladimir I. Falko, and R. J. Haug. Correlation-function spectroscopy of inelastic lifetime in heavily doped GaAs heterostructures, Phys. Rev. B 64, 155314 (2001).

[80] Carleton H. Seager, GRAIN BOUNDARIES IN POLYCRYSTALLINE SILICON, Ann. Rev. Mater. Sci. 15, 271-302 (1985).

[81] C. R. M. Grovenor, Grain boundaries in semiconductors, J. Phys. C: Solid State Phys. 18 40793119 (1985).

[82] Edgar Bonet, Mandar M. Deshmukh, and D. C. Ralph, Solving rate equations for electron tunneling via discrete quantum states, Phys. Rev. B 65, 045317 (2002).

List of Tables

List of Figures

Acknowledgment

I would like to thank my PhD supervisor Prof. Dieter Kern for giving me the opportunity to do PhD in his group. I would like to thank him for helping me during my transition from India to Germany with traveling, housing in Germany and other administrative issues. During my PhD work I had very interesting and inspiring discussions with him. I would also like to thank Prof. David Wharam for co-supervising my thesis. I would like thank him for his valuable and motivating discussions and suggestions during the PhD period.

During the PhD work, I got to interact with the AFSID project partners, namely Marc Sanquer, Xavier Jehl, Maud Vinet, Romain Wacquez , Mathieu Pierre, Benoit Roche, Marco Fanciulli, Enrico Prati, Arjan Verduijn, Sven Rogge, David Williams, Paul Chapman and David Jamieson which was very useful for this work. I would like to thank Matthias Ruoff and Stefan Jauerneck for technical assistance with the measurement set-up and discussion of the results. I would like to thank Danial Schefzyk for his help with dilution refrigerator and simulations and also providing small but very useful programs. I would like to thank all the group members for such a nice working atmosphere which made my PhD work so much fun.

I would like to thank my family for constant support, valueable suggestions and encouragement, especially my mother and father for their love and understanding. I would like to thank my brothers Sagar and Vishal Kotekar-Patil for listening patiently to me during difficult times and making some useful suggestions. Without them this work was not possible. Thanks to Swara and B.M. Being away from home is not always easy. I am very lucky to find Kathrin Stauber (better known as “J”). I thank her for her constant support, patience and encouargement during the PhD work. I would also like to thank all my Indian friends with whom I had really fun time here in Germany. Last but not least, I would like to thank Stauber family for introducing me to the German culture and their hospitality during this period.

Eidesstattliche Versicherung

Ich erkläre hiermit, dass ich die zur Promotion eingereichte Arbeit mit dem Titel "**Single Electron Transistors in CMOS Compatible Silicon MOSFETs**" selbständig verfasst, nur die angegebenen Quellen und Hilfsmittel benutzt und wörtlich oder inhaltlich ubernommene Stellen als solche gekennzeichnet habe. Ich versichere an Eides statt, dass diese Angaben wahr sind und dass ich nichts verschwiegen habe. Mir ist bekannt, dass die falsche Abgabe einer Versicherung an Eides statt mit Freiheitsstrafen bis zu drei Jahren oder mit Geldstrafe bestraft wird.

Weiterhin erkläre ich, dass bisher kein Promotionsversuch unternommen wurde.

Tübingen, den ______________ ________________________________

List of Publications

Papers

1. Few Electron Limit of n-type Metal Oxide Semiconductor Single Electron Transistors Enrico Prati, Marco De Michielis, Matteo Belli, Simone Cocco, Marco Fanciull, Dharmraj Kotekar-Patil, Matthias Ruoff, Dieter P. Kern, David A. Wharam, Arjan Verjuijn, Giuseppe Tettamanzi, Sven Rogge, Benoit Roche, Romain Wacquez, Xavier Jehl, Maud Vinet, Marc Sanquer, Nanotechnology 23 (2012) 215204.
2. Charge Granularity in Single electron transistors with Polysilicon gates D. Kotekar-Patil, M. Ruoff, S. Jauerneck, D. Wharam, D. P. Kern, Xavier Jehl, Romain Wacquez, M. Sanquer, Proceedings of 13th International Conference on Ultimate Integration of Silicon ULIS (2012).
3. Mass production of Silicon MOS-SETs: Can we live with nano-devices' variability? X. Jehl, B. Roche , M. Sanquer , B. Voisin , R. Wacquez , V. Deshpande , B. Previtali , M. Vinet, J. Verduijn , G. C. Tettamanzi , S. Rogge , D. Kotekar-Patil , M. Ruoff , D. Kern , D.A. Wharam , M. Belli , E. Prati , M. Fanciulli, Proceedings of the FET2011 conference, Computer Science, Elsevier eds. 2011.
4. Growth and Characterisation of Quantum Well infrared photodetectors (QWIPs) materials by MBE, Sen Mathews, Amit Shah, Dharamraj Patil, Mahesh Gokhale, S.C. Purandare, Rajeev Shenoi, Ajit Barve, Sanjay Krishna, K. Chalapathi, Arnab Bhattacharya, and B. M. Arora, Proceedings of International Workshop on Physics of Semiconductor Devices 2009.

Posters

1. Charge Granularity in Single electron transistors with Polysilicon gates, D. Kotekar-Patil, M. Ruoff, S. Jauerneck, D. Wharam, D. P. Kern, Xavier Jehl, Romain Wacquez, M. Sanquer, Ultimate Integration on Silicon 2012, Grenoble, France.
2. Floating gate effect in CMOS single electron transistor, D. Kotekar- Patil, M. Ruoff, S. Jauerneck, D. Wharam, D. P. Kern, Nanoresonance 2011, Blaubeuren, Germany.
3. Triple dot structures from CMOS-compatible SOI-FETS, D. Kotekar- Patil, M. Ruoff, S. Jauerneck, D. Wharam, D. P. Kern, M. Sanquer, M. Vinet, DPG spring conference 2010, Dresden, Germany.
4. Geometry effects on Coulomb charging in CMOS-compatible SOI-SETs, Matthias Ruoff, D. Kotekar-Patil, Stefan Jauerneck, David Wharam, Dieter Kern, Marc Sanquer, Maud Vinet, DPG spring conference 2010, Dresden, Germany.
5. Low Temperature Coulomb Anomaly in CMOS compatible Silicon Quantum Dots, Stefan Jauerneck, Matthias Ruoff, D. Kotekar-Patil, David Wharam, Di-

eter Kern, Marc Sanquer, Maud Vinet, DPG spring conference 2010, Dresden, Germany.

Curriculum Vitae of Dharmraj Kotekar-Patil

Personal Information:

Date of Birth: 9th April 1984

Place of birth: Hubli Dharwad, Karnataka, India

Educational Background:

2000: St. Aloysius High School, Mumbai, India

2002: St. Andrews Junior College, Mumbai, India

2002-2005: Bachelor of Science in Physics, University of Mumbai, Mumbai, India

2005-2007: Master of Science in Physics, University of Mumbai, Mumbai, India

2009-2013: PhD in Physics, University of Tuebingen, Tuebingen, Germany

Research Experience:

2007-2009: Junior Research Fellow at Society for Applied Microwave Electronics Engineering & Research, Mumbai, India.